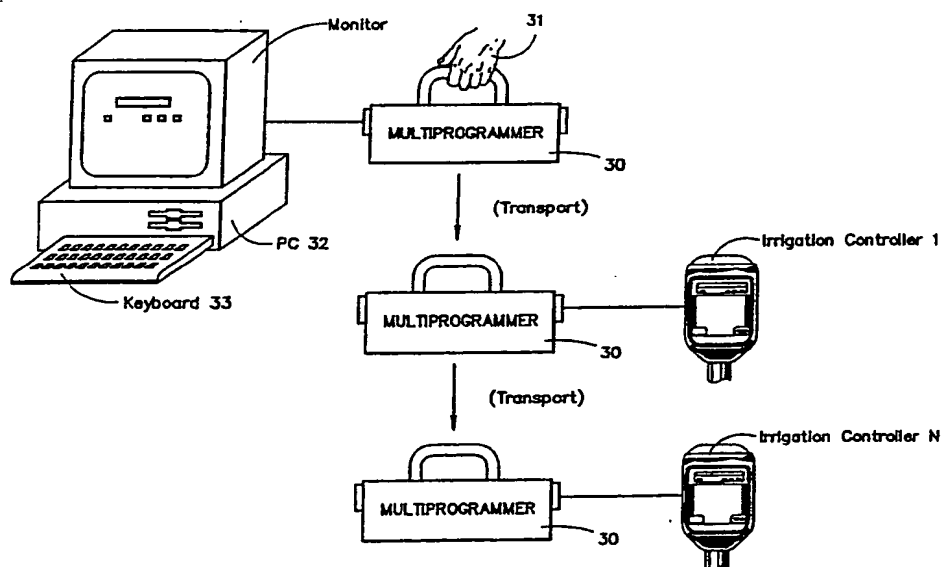




## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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<b>(21) International Application Number:</b> PCT/US89/04403 <b>(22) International Filing Date:</b> 4 October 1989 (04.10.89) <b>(30) Priority data:</b> 255,150                      4 October 1988 (04.10.88)                      US <b>(71) Applicant:</b> SOLATROL, INC. [US/US]; 11055 Roselle Street, San Diego, CA 92121 (US). <b>(72) Inventors:</b> NIELSEN, Wyn, Y. ; 3918 La Jolla Village Drive, La Jolla, CA 92037 (US). LUCK, Jonathan, M. ; 6537 Reflection Drive, Apartment 210, San Diego, CA 92124 (US). <b>(74) Agent:</b> FUESS, William, C.; Dressler, Goldsmith, Shore, Sutker & Milnamow, Ltd., 11300 Sorrento Valley Road, Suite 200, San Diego, CA 92121 (US).		<b>(81) Designated States:</b> AT (European patent), AU, BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).  <b>Published</b> <i>With international search report.</i>

**(54) Title:** DISTRIBUTED MULTIPLE IRRIGATION CONTROLLER MANAGEMENT SYSTEM**(57) Abstract**

Separate, but related, firmware programs for multiple microprocessor-controlled irrigation controllers (1) that are interrelated in their control of irrigation within an irrigation system are generated off-line at a personal computer (32). The programs are downloaded into a transportable memory device (30) that holds sixty-four separate programs. The memory device (30) is transported to each irrigation controller (1) and plugged to a digital communication channel (15). The device automatically identifies itself to the controller (1), and vice versa. The appropriate program is automatically uploaded from the device (30) to the controller (1). The controller's (1) old program and its historical irrigation record data is loaded into the device (30) and delivered to the personal computer (30) for validation and analysis. A wireless remote test command assembly (61), an extension maintenance panel (42), or a radio-link central module (50) may be alternatively connected to the controller's digital communication channel (15).

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DISTRIBUTED MULTIPLE IRRIGATION  
CONTROLLER MANAGEMENT SYSTEM

BACKGROUND OF THE INVENTION

5     1.0     Field of the Invention

The present invention concerns the coordinated programming and test control of multiple independent, but irrigation-function interrelated, programmable electronic irrigation controllers within an irrigation system.

10    2.0     Background of the Invention

Large irrigation systems, such as those for golf courses and parks, typically use many dozens of independently operative irrigation controllers. Each irrigation controller controls a number of valves that gate the flow of irrigation water, typically to eight valves per controller. Because each irrigation controller must be electrically wired to all valves that it controls, it is infeasible to have the many hundreds or thousands of valves in a large area irrigation system controlled by a single controller.

20           Although each irrigation controller is independent in its operation, the irrigation control exercised by multiple irrigation controllers is typically interrelated, and must be coordinated. This is because the piping of irrigation water to the stations, or valves, of a number of irrigation controllers is usually in series, one station to the next. A fundamental rule of irrigation control is that only such numbers of irrigation stations should be simultaneously enabled for irrigation watering as do not, resultant to the drop on hydrostatic pressure and flow caused by each "on" station, adversely affect irrigation watering pressures, flows, and patterns at any one(s) of the simultaneously enabled stations. Because most irrigation piping is of minimal diameter and cost consonant with the water flow and pressure requirements of a single irrigation station, application of the rule normally requires that only one irrigation station should be enabled any

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one time.

Enabling one only irrigation station, or valve, to be on at one time among all the valves controlled by a single irrigation controller is merely a matter of the setup, or programming, of that one irrigation controller. However, if  
5 separate and independent irrigation controllers must be coordinated, as is typically required due to the plumbing of irrigation water, then matters become more difficult. A programmer/user of interrelated irrigation controllers must  
10 understand the hydrodynamic relationships of the valves controlled by each. These relationships may be several and may be at several hydrodynamic levels within a large irrigation system. In accordance with this understanding, the programmer/user must program irrigation at each irrigation  
15 controller in consideration of his/her programming of the other irrigation controllers.

Even when the necessary coordination of irrigation control programming is kept track of on paper, its actual implementation is difficult and fraught with error. The  
20 irrigation controllers themselves are typically difficult and time consuming to program. They are required to be programmed where located, meaning in the field. The weather conditions under which the irrigation controllers must be programmed, and the caliber and diligence of the workers that must tend to the  
25 programming, are not always good. Considerable difficulty of coordination between irrigation controllers is experienced. It is hard to affect any appreciable change at any one controller until all controllers are reasonably well coordinated.

30 These difficulties tend to impart a great deal of undesired rigidity to the entire irrigation programming process. The system wide reprogramming of an irrigation system because of variations in rainfall, seasonal variations, changed site requirements and numerous other reasons is often  
35 undesirably foregone simply because it is excessively difficult

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to plan, setup, or repeatedly setup coordinated irrigation control.

One previous approach in dealing with the difficulties in the coordinated setup, or programming, of multiple independent but functionally interrelated irrigation controllers within a single irrigation system has been based on the establishment of one master and several satellite irrigation controllers. The master irrigation controller communicates with its satellite irrigation controllers to sequence their respective operations. Flexibility in scheduling is typically constrained by the nature of the sequential control of the satellite irrigation controllers. The expense of a wired communication network is incurred. The problem of coordinating multiple interrelated irrigation controllers is simply moved to a higher level because multiple master irrigation controllers may themselves now require coordinated set-up, now at typically increased complexity, one to another.

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## SUMMARY OF THE INVENTION

The present invention contemplates (i) generating one or more programs for one or more potentially interrelated irrigation controllers at a central computer, (ii) downloading the one or more programs from the central computer into a transportable memory device, (iii) transporting, and communicatively connecting, the transportable memory device to each one of the one or more potentially interrelated irrigation controllers in series, and (iv) uploading a program from the transportable memory device into each one of the one or more irrigation controllers.

The central program generation preferably transpires on a digital computer, typically on a personal computer. The computer permits the assembly (or compilation) of the programs that will be executed by the actual irrigation controllers. Each irrigation controller preferably contains a

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microprocessor, nominally a type 6502 contained within an Application Specific Integrated Circuit, and executes firmware programs to effect irrigation control. The personal computer generates these firmware programs by running commercially available assemblers (or compilers) for this popular microprocessor. These programs are individualized as required or desired to each irrigation controller.

Moreover, the personal computer is preferably programmed so as to emulate the irrigation controllers both individually and collectively. This emulation is particularly of the manual input control and, in the form a display, the valve control and/or displays that would be produced by an actual irrigation controller as it would execute a particular actual program. The personal computer does not produce control signals to valves during its emulation of an irrigation controller, although it could do so. It is sufficient for the purposes of the present invention that the personal computer should merely emulate the responses of an irrigation controller as it executes a particular program.

Because each irrigation controller is entirely controlled by only four pushbutton switches (OK/YES, NO, HELP, and STOP), because each controller generates only a modest number of relatively short messages and the on/off control of only eight valves, and because each controller runs firmware that is easily emulated in execution by the personal computer meanwhile that the controller's emulation need not be (and is usually not) conducted in real time, the emulation of one or more irrigation controllers by the personal computer is straightforward. This simultaneous emulation of one or more controllers permits debug of the control program of any one controller and, importantly, visibility (on the screen of the personal computer's monitor) of the diurnal irrigation control arising from multiple interrelated controllers. A central programmer's task in coordinating a number of interrelated irrigation controllers for the control of irrigation within a

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single irrigation system is thus much facilitated.

The transportable memory device preferably interfaces to the personal computer by a standard digital serial interface type RS-232C, and to each irrigation controller by a custom digital interface. The custom digital interface is functionally distinguished by starting automatically upon physical electrical connection of the memory device and an irrigation controller, by having the controller automatically identify itself to the memory device and vice versa, and by automatically uploading the appropriate program from the memory device into each individual controller.

The memory device can preferably carry up to sixty-four (64) complete irrigation control programs simultaneously. It preferably employs the same microprocessor (type 6502 contained within an Application Specific Integrated Circuit) that is also used within the irrigation controller. The automated, microprocessor-managed, interchange of unit identities and the automated transfer of an appropriate program minimizes any required human involvement and/or skills at the controllers' field sites, and permits the complex programmed setup of many irrigation controllers to be quickly and easily accomplished by unskilled field workers.

The irrigation controllers each keep a time-of-day clock. Each controls the conduct of irrigation in accordance with schedules computed by its microprocessor from execution of its individually associated firmware program. Because the programs that were generated at the central source are coordinated for the timed control of irrigation at many dozens or hundreds of stations (valves) within an irrigation system, the actual timed irrigation control effected by the irrigation controllers is also so coordinated. In particular, a number of physically separate and independent irrigation controllers that are interrelated in their required functional control of irrigation may readily be coordinated so as to respond as a single virtual controller. For example, three irrigation

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controllers controlling eight stations each may readily be coordinated in operation to act as one virtual controller controlling twenty-four stations. The concept of virtual irrigation controllers -- which virtual controllers are readily  
5 created and programmed at the personal computer -- much facilitates the ease with which a programmer may think about the programming of coordinated irrigation control within an irrigation system.

The present invention further contemplates that the  
10 irrigation controllers should load information into the portable memory device, and that this information should be carried back to the central station personal computer to be offloaded for analysis, verification, and/or printout. The loaded information commonly comprises both the existing,  
15 previous, firmware program to that one being uploaded (if any is) plus data in the form of actual historic operational occurrences (normally for the prior 30 days). Ability to recover the existing irrigation controller firmware program permits the study and analysis of programs installed in the  
20 field, or the verification whether or not programs previously believed to have been installed were so installed in fact. The ability to recover actual historical data permits analysis of irregular occurrences, improvement of irrigation watering amounts and schedules in accordance with actual site conditions  
25 (especially as sensed by optional moisture sensors), and validation of proper irrigation system performance.

The present invention still further contemplates that other devices than the transportable memory device should be selectively connectable to the custom digital interface of the  
30 irrigation controller. Each device identifies itself to the irrigation controller and to its microprocessor operating under firmware program control. The irrigation controller thus normally requires no manual intervention other than physical connection of each device in order to cooperatively  
35 interoperate with such device.



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A portable maintenance panel extender device connects a substitutionary or additional maintenance panel for that maintenance panel that is customarily under a cover plate of the irrigation controller. One benefit so derived is the capability of placing the irrigation controller, which is light-energized, upon a high pole where it is substantially immune from vandalism while maintaining the connection for this portable extended maintenance panel, normally within a strong locked enclosure, at a height whereat it may be conveniently accessed.

A radio-linked central programming system for multiple irrigation controllers uses a radio transceiver that is connected to each controller's digital interface port. A central, or mobile radio transceiver sends and receives controller specific information at prescheduled times, typically diurnally. The irrigation controller typically does not have much stored energy to power its connected radio transceiver. The radio transceiver is correspondingly inactive at all times save for prescheduled time intervals when an individual controller may be addressed.

A wireless remote test command system permits manual test operation of the valves connected to an irrigation controller. The valves that are connected to an irrigation controller may generally be locally exercised through the maintenance panel of the irrigation controller. In the remote test command system, a self-powered transceiver is temporarily plugged into the digital interface of the irrigation controller. A hand-held transceiver that is carried by an installer or maintenance person is used to test the operation of valves (and the readings of optional soil sensors, if implemented) without the necessity of physically returning to the controller. Considerable time and walking may be saved in testing for sprinkler and pipe performance, for leaks or obstructions, in checking soil sensor performance, and in validating all repairs.

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These and other aspects and attributes of the present invention will become increasingly clear upon reference to the following drawings and accompanying specification wherein:

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## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a pictorial diagram of an irrigation controller in accordance with the present invention;

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Figure 2 is a block diagram of an irrigation system in accordance with the present invention including the irrigation controller illustrated in Figure 1;

Figure 3 is a pictorial diagram of a multiprogrammer unit in accordance with the present invention in use to transport programs to the irrigation controller;

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Figure 4 is a pictorial diagram of a maintenance panel extender to the irrigation controller;

Figure 5 is a pictorial diagram of a radio-linked central programming system for communication with irrigation controllers;

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Figure 6 is a pictorial diagram of a remote test command system for exercising and testing irrigation controllers;

Figure 7, consisting of Figure 7a through Figure 7h, is a schematic diagram of the preferred embodiment of an irrigation controller in accordance with the present invention;

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Figure 8 is a block diagram of a first, U1, Application Specific Integrated Circuit (ASIC) used in the preferred embodiment of an irrigation controller in accordance with the present invention;

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Figure 9a is a simplified electrical schematic diagram of the sampling capacitor array and switches used in ASIC U1;

Figure 9b is a simplified electrical schematic diagram of a sampling comparator used in ASIC U1;

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Figure 9c is a simplified electrical schematic diagram of a step-up DC-to-DC Converter used in the switching regulator of ASIC U1;

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Figure 10, consisting of Figure 10a through Figure 10d, is a block diagram of a second, U2, Application Specific Integrated Circuit (ASIC) used in the preferred embodiment of an irrigation controller in accordance with the present invention.

5           Figure 11 is a schematic block diagram of a preferred embodiment of the multiprogrammer previously seen in Figure 3.

Figure 12 is a detail schematic diagram of the preferred embodiment of the multiprogrammer previously seen in Figures 3 and 11.

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## DESCRIPTION OF THE PREFERRED EMBODIMENT

1.0 The Preferred Embodiment System of the Invention  
Includes a Light-Energized Irrigation Technology  
Controller

5 The present invention is embodied in a system for the programming and test control of an irrigation controller. The irrigation controller is preferably light-energized for the control of irrigation through eight stations, or valves, of up to 128 total cycles per day. The irrigation controller is  
10 spoken of as being "light-energized" and (along with the irrigation valves that it controls) to embody "Light-Energized Irrigation Technology" (LEIT). This description is in lieu of describing, for example, the controller to be "solar powered" because it employs an extremely small area light (solar)  
15 collector. Resultant to the small energy collected, the controller uses extremely little energy for all irrigation functions, including control of up to eight (8) valves. The acronym LEIT when applied to irrigation controllers is a trademark of Solatrol, Inc. (assignee of the present  
20 invention), i.e., LEIT™ Irrigation Controllers.

1.1 Operational Specification of the Preferred Embodiment  
of an Irrigation Controller in Accordance with the  
Present Invention

25 No electrical power input is required. Light energy required is 0.4 milliwatts/sq cm incident light for a minimum of 7 hrs/day. This is approximately equivalent to one tenth of the amount of light at 55° northern latitude (e.g., in Canada) on a cloudy winter's day.

30 The power for the controller's display (when actuated) is derived from a POWERKEY™ (trademark of Solatrol, Inc.) power source. The POWERKEY™ power source packages a 9-volt alkaline battery that is used to energize the Liquid Crystal Display (LCD) of the controller during installation and programming.

35 The signal output of the controller to its controlled valves is 3.5 volts DC, 0.04 amps for .04 seconds. No circuit

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breaker and no transformer are required.

Up to 8 valves (including up to 4 Master Valves) may be connected to each controller. Up to 8 electronic soil moisture sensors or optionally, other compatible electronic sensing devices, may also be connected to each controller.

A user-defined emergency backup program and critical system parameters are stored in non-volatile memory in case of memory loss from prolonged light interruption; no batteries are needed.

10 1.2 The Preferred Embodiment of a LEIT™ Irrigation Controller Interfaces with Other Devices in Order to Be Remotely Programmed and/or Controlled

The preferred embodiment of a LEIT Irrigation controller in accordance with the present invention interfaces with other devices for the loading of irrigation control programs and the manual exercise of irrigation valves and sensors.

A POWERKEY™ (trademark of Solatrol, Inc.) power source is a combination keyring and keyfob-cased battery for powering the irrigation controller and its display during programming and/or interactive operation. The POWERKEY™ power source is manually plugged to the controller. It provides power to the controller for its very first use, and thereafter during each episode of the programming/parameterization of the controller's operation and/or the reviewing of data in the controller's memory. The POWERKEY™ power source also provides power to the built-in illumination of the controller's display and control switches. The power source that is used during operation of the controller to control irrigation may be the POWERKEY™ power source if it is still pluggably attached (an abnormal condition), but is normally light (even extremely dim light, such as moonlight) that falls upon the controller.

A Multiprogrammer™ unit plugs into the digital interface of the controller for uploading and downloading the irrigation watering program that is executed by the controller.

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The Multiprogrammer unit simultaneously holds the programs for up to 64 controllers.

5 A remote test command assembly mounts in position as a replacement controller face-plate. It plugs into the digital interface of the controller and receives signals from a hand-held transceiver carried by a maintainer in order to allow wireless remote "manual" operation of the controllers valves and sensors. This remote operation characteristically occurs while the maintainer inspects the valve or sensor locations.

10 An extension maintenance panel substitutes for, or replicates (as is specified and configured during build of the irrigation controller) the normal maintenance and control panel of the irrigation controller. The extension maintenance panel is remotely situated from the controller in a position where  
15 it may be accessed. The controller is typically located atop a high pole so as to collect light while being isolated from damage due to accident or vandalism. The extension maintenance and control panel contains only four switches and a display. It interfaces to the controller's digital interface.

20 A radio-link module mounts permanently to the controller at its digital interface. The module acts as a transceiver for wireless communication between the controller and a radio-link central system. The same program and data information is normally communicated by radio as is  
25 alternatively carried in the Multiprogrammer unit.

Only one of the Multiprogrammer unit, the remote test command assembly, or the radio-link central module attaches to the irrigation controller at its digital interface at one time. Each device identifies itself to the controller, and the  
30 individual controller (of which there may be many in an irrigation system) is likewise identified to the device. The Multiprogrammer unit, the extension maintenance panel, the radio-link module and the remote test command assembly provide their own power.

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The controller-mounted transceiver of the radio link module is energized but momentarily on a daily schedule. Messages communicated by radio normally include operating programs to be downloaded into the controller, or historical data to be uploaded to the central station. If a message is to be passed, then a controller's radio-link module will remain energized for the duration of the message. Otherwise the powering of the radio link is only momentary.

Up to 8 optional soil moisture sensor units can connect to the controller to give precise irrigation system control based on readings of available soil moisture tension, or optionally, percentage soil saturation.

### 1.3 Features and Benefits of the Preferred Embodiment of a LEIT Irrigation Controller in Accordance with the Present Invention

The preferred embodiment of an irrigation controller in accordance with the present invention is light-energized with a built-in incident light collector. It exhibits sufficient energy storage to drive a custom CMOS ultra-low-power microcomputer with 32K RAM memory and to cycle up to eight (8) ultra-low-power irrigation valves up to sixteen (16) times each per twenty-four (24) hour period. This provides complete independence from any need for AC power, saving on energy and installation costs and permitting the controller to be located closer to the valves.

An easy to read two-line LCD display with automatic prompting is implemented. The user is guided through the programming process with easy to understand two-line "prompts," thus substantially eliminating confusion, mistakes, and requirements to repeatedly reference printed or human authority.

Two-button programming with "best guess" defaults is used for all settings. All programming is done by answering simple questions with OK or NO answers. The controller automatically gives the user "best guess" defaults where

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applicable.

5 An on-line help feature gives directions and information for each operational mode and parameter insertion. These on-line help messages are available at any time by pressing a HELP key.

10 The design is modular in that multiple 8-valve-station controller units can be integrated together. The individual 8-valve-station controller units can be networked together into optionally radio-linked centrally controlled systems, or, alternatively, multiple unrelated controllers on various sites can be centrally managed by optional multi-programming equipment.

15 Each of the 8 stations for a single controller unit can be independently programmed within one of six different runtime modes (Mini, Autosplit, Ration, One-Time, and Special. This gives the Irrigation Controller great programming flexibility. Options for (i) simplified "Mini" setups, (ii) "Autosplit" setups with automatically programmed split cycles and sequential non-overlapping operation, (iii) "Ration" setups for odd/even (day of month) water rationing, (iv) "ISC" setups with complete independence between stations, (v) "Special" setup for lights, fountains, and pump-start relays, (vi) periodic or one-time "Add-on Soak Cycle" setups, and (vii) for multiple "Add-on Syringe Cycle" setups are implemented.

25 Controller timing control of the irrigation valves is from 1 minute to 240 minutes in one minute increments. Thus one minute precision in starting or stopping irrigation is combined with the ability to set watering durations of up to 4 hours for each start time. One-time or periodic "soak cycles" can have a duration of up to 8 hours.

30 A calendar is maintained based on "perpetual calendar" data in permanent memory. Schedules may be established for specific days or every "so many" days. This permits flexible day cycles for irrigation, and allows different stations to operate on different day cycles.



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Up to 128 automatic starts per day are enabled, thereby meeting the most demanding applications.

5       The controller's split cycle capability permits watering times to be split into up to 16 substantially equal increments. This minimizes runoff and puddling by splitting the programmed watering duration into shorter cycles each of which is separated by a programmable minimum "off" time.

10       A System Budgeting Factor of 10 to 200% acts to determine the numbers of split cycles. The System (water) Budgeting Factor increases or decreases the number of split cycles instead of acting as a total duration multiplier which can lead to runoff and puddling. Monthly budgeting with pre-set default values for each month is also available. This allows an entire year's scheduling to be set up.

15       An Integrated Moisture Sensor control with programmable "wet" and "dry" trigger levels is optionally implemented for each valve station. This keeps the soil moisture level for each valve within the optimal range for the growth of the type of vegetation being watered by that valve, instead of merely  
20       using the optional moisture sensors as switches to override cycle starts.

      Automatic sequential program generation permits "Excluded Time Intervals". The controller automatically generates a sequential matrix of start times for all active  
25       valves and split irrigation cycles based on user input for determined total watering durations by valve, either site information selection or operator entered number of split cycles, and on any user-defined "Excluded Time Intervals" when no watering is desired.

30       For very simple applications a "Mini" setup is available. This simple setup mode is extremely easy to use, and it is designed for applications where some of the more sophisticated features of the controller are not needed.

      Another option, the "Special setup", can be used for  
35       control of non-valve devices such as pumps, or lighting

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equipment.

One-time or periodic "Soak" cycles can be overlaid on any regular watering program. This feature can be used for watering in fertilizer, for periodically deep watering trees and shrubs in turf areas, and for periodically leaching salts in drip applications.

Multiple daily cooling or frost-wipe "Syringe" cycles can be overlaid on any regular watering program for any pre-programmed month(s) when needed. These cycles help prevent wilting and scorching of plant materials during hot summer months or damage from freezing or morning dew in cold weather months.

Even and odd days can be automatically excluded as watering days in the "Ration" setup mode. This allows for odd/even water rationing schedules to be easily programmed where this is mandated by law.

A programmable "Delay Start" permits watering to be suspended for up to 14 days during rainy weather, and at the end of the programmed "Rain Delay" the regular watering schedule will automatically resume.

A special "View Info" mode allows the user to review all settings or to view an event report which displays the controller history and current operational setup. This permits the user to easily review the current controller settings or to view a list of the last 128 events (watering cycles, program changes, etc.) in chronological order starting from the earliest event.

Built-in wire continuity and short testing, system self-test and report functions are implemented. The user is alerted if shorted or open valve wires exist, and the unit performs a self-diagnostic test when requested.

A "Test Sequence" allows each valve to be operated in sequence for one to thirty minutes. This allows the irrigation system to be easily periodically tested. A STOP key lets the operator immediately stop the test sequence if broken

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sprinklers or pipes are found.

Both valve stations and sensors can be operated automatically, semi-automatically, or manually. In semi-automatic mode, all or selected valves can be run once using  
5 the "One-Time" setup. This allows the user to do a one-time soak for watering in fertilizer or new plantings. The controller then automatically reverts to the automatic "Run" mode.

10 Three level access codes provide security and render the controller useless if stolen. Separate codes for gardeners, supervisors, and factory personnel insure that only authorized individuals can change the controller settings, and that codes can be easily changed as operating personnel change.

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## 2.0 Overview of the Preferred Embodiment of An Irrigation Controller

The preferred embodiment of an irrigation controller in accordance with the present invention uses Light Energized Irrigation Technology (LEIT™). It can operate with the amount of incident light available in northern latitudes on a worst-case cloudy winter's day without needing any of the batteries, external solar panels, or the A.C. power connections required for traditional controllers. It is also extremely flexible and versatile in its operation.

A diagrammatic view of the preferred embodiment of the controller, with its cover plate removed and operator's panel area exposed, is shown in Figure 1. Controller 1 is typically attached to post 2. A photovoltaic device 10 (not shown) is located under transparent lid 11 to case 12.

Various electrical connectors are presented. A valve connector block 13 permits electrical connection by wires (not shown) to up to eight (8) electromagnetically actuated valves. A control key socket 14 accepts a pluggable POWERKEY™ power source (not shown), being a 9 vdc battery suitably packaged so as to plug into socket 14. A digital accessory connector 15 permits communication connection to a Multiprogramming unit (not shown) that may upload and download programs into the controller 1 (among other alternative ways of programming controller 1). The connector 15 is a standard type, and may, under firmware control within controller 1, interface to further devices. A sensor connector block 16 permits connection of up to eight (8) optional soil moisture sensors or other sensing devices. These soil moisture sensors, and the control proceeding therefrom, are not taught within this specification for being unimportant to the present invention.

A control panel 20 contains a liquid crystal display (LCD) 21 for showing information, questions, and directives. The control panel 20 also contains pushbutton switches 22-25. A STOP switch 22 stops the present controller 1 operation and

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turns off any valves previously turned on. A HELP switch 23 causes the controller 1 to display more information and/or instructions, keyed to the current operation or displayed questions, in LCD 21. The NO switch 24 and the OK switch 25 are used to answer controller-presented questions about the installation and the parameters of irrigation (e.g., the watering schedule) and to enable selectable readout of controller stored data.

The controller 1 is controlled in its operation by firmware running on a special Application Specific Integrated Circuit (ASIC) that includes a microprocessor. The explanation of the controller 1 hardware is contained in major sections 3-5 of this specification. This major section 2 deals with the user interface to controller 1, and serves to show its many unique aspects in accordance with the present invention.

The term "programming" used throughout this specification includes actions performed at the operator interface to the controller 1 -- actions normally but not necessarily performed in the field -- by which the controller 1 is parameterized and directed in its programmed operation. The firmware itself is, of course, also "programmed". In some cases the act of "programming" at the operator's panel will alter the flow, as well as the parameters used, within the firmware; thus constituting a form of "programming" at the process control level. The word "programming" is used to refer to the total compendium of operator/programmer interface to, and control of, irrigation controller 1. The word includes actions more exactly thought of as parameterization (typically done in the field), as well as actions more exactly thought of as coding (typically done in the factory or depot).

## 2.1 Overview of the Preferred Embodiment of an Irrigation System

A preferred embodiment of an irrigation control system in accordance with the present invention is shown in Figure 2.

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An irrigation controller 1 (previously seen in Figure 1) operates under control of MICROPROCESSOR U2 (partial) executing programmed firmware that is resident in memories types ROM U4, RAM U5, and EE U9. The MICROPROCESSOR U2 (partial) communicates with MANUALLY OPERABLE KEYS 22-25 (previously seen in Figure 1) for receipt of data and control. It interfaces with DISPLAY 21 (previously seen in Figure 21) for the display of questions, parameters, and help messages to a human user/programmer (as detailed in previous section 2.0).

The MICROPROCESSOR U2 (partial) of irrigation controller 1 optionally communicates externally through a SENSOR INTERFACE 26 of plugjack 16 (shown in Figure 1) to up to eight MOISTURE SENSING UNITS (optional) 27a-27h (shown in phantom line). This optional communication is the purpose of sensing soil moisture at up to eight locations. The MICROPROCESSOR U2 (partial) communicates through VALVE INTERFACE 28 of plugjack 13 (shown in Figure 1) to up to eight electromagnetically actuated CONTROL VALVES 29a-29h (shown in dashed lines). This communication is for the purpose of gating the flow of pressurized water from WATER SUPPLY 30 through a selected one of CONTROL VALVES 29a-29h at any one time to a corresponding one of WATERING HEADS 31a-31h (shown in dashed line).

The MICROPROCESSOR U2 (partial) may optionally communicate through plugjack 15 (shown in Figure 1) to OTHER DEVICES 32 (shown in phantom line) for purposes of receiving the download of firmware programs, parameters, and/or commands. This interface need not be enabled to operate the irrigation controller 1, which in a preferred embodiment comes from the factory with that control program that is appendicized to this specification within its ROM memory U4 and EE memory U9, and which in the preferred embodiment may have all necessary parameters and control entered through MANUALLY OPERABLE KEYS 22-25. Indeed, if necessary firmware could be entered into controller 1 through it's MANUALLY OPERABLE KEYS 22-25. The

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digital interface to OTHER DEVICES 32 simply represents a less tedious way of communicating.

5 The preferred embodiment of the controller 1 normally derives all its power, and all power for MOISTURE SENSING UNITS 27a-27h and CONTROL VALUES 29a-29h, during quiescent operation both day and night from radiant light energy impinging upon RADIANT ENERGY CONVERTING UNIT (includes ASIC U1) that comprises each of PVM1, U1, and ASSOCIATED CIRCUITRY. "PVM" stands for photovoltaic module and "ASIC" stands for  
10 application specific integrated circuits. All "U" designations stand for integrated circuit chips that may be referenced in Figure 3 (to be discussed).

The preferred embodiment of controller 1 is powered during its operation to accept user programming not by the  
15 RADIANT ENERGY CONVERTING UNIT PVM1, U1, and ASSOCIATED circuitry but rather by electrical connection through plugjack 14 (shown in Figure 1) to the POWERKEY™ PLUGGABLE BATTERY ENERGY SOURCE 33. This SOURCE 33, normally not a part of irrigation controller 1 during its quiescent operation, is  
20 shown neither in shadow line for being optional, nor in dashed line for being related to the controller 1 of the present invention but not part thereof. Rather, the POWERKEY™ PLUGGABLE BATTERY ENERGY SOURCE is shown in solid line in order to illustrate that for the purposes of programming the  
25 controller in accordance with the present invention it must be present.

This required presence is because the SOURCE 33 supplies the greater power that the MICROPROCESSOR U2 (partial) needs to exit the predominantly somnolent (inactive) state that  
30 it only intermittently and momentarily leaves to effect irrigation control in accordance with the schedules, and to assume a high duty cycle at operation. The SOURCE 33 also supplies the power requirements of MANUALLY OPERABLE KEYS 22-25 and of DISPLAY 21 during user programming. Although the  
35 energy storage within the RADIANT ENERGY CONVERTING UNIT might

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suffice to permit user programming, it is unwise to deplete this energy storage to an undetermined amount (dependent on the length and adeptness of user programming) -- especially at night when no energy recovery is possible and especially when the controller is programmed to immediately begin controlling irrigation cycles. Instead, the SOURCE 33 actually charges the energy storage means within the RADIANT ENERGY CONVERTING UNIT, and always leaves the controller 1 fully powered and ready to control irrigation of the end of a user programming sequence.

## 2.2 The Multiprogramming System

The preferred embodiment of a system for delivering programs from a central program generation device to one or more independent irrigation controllers is pictorially illustrated in Figure 3.

A MULTIPROGRAMMER unit 30 is carried by a maintenance person 31. It contains all the programming instructions for up to 64 controllers. The MULTIPROGRAMMER unit 30 plugs into one of the IRRIGATION CONTROLLERS 1 through N whereupon the controller identifies itself to the MULTIPROGRAMMER unit and receives any new programming instructions intended uniquely for that controller. During the same communication episode the MULTIPROGRAMMER unit 30 receives and stores existing programs and history data from the controller. Later, back at the maintenance office, the MULTIPROGRAMMER unit 30 plugs into any personal computer PC 32 and reads out this information for verification and/or printout.

The PC 30 runs software used for programming the IRRIGATION CONTROLLERS, and for emulating their function. The preferred software is the "6502 ASSEMBLER" for the 6502 microprocessor chip available from 2500AD Software, Inc., 17200 E. Ohio Drive, Aurora, Colorado 80017. The PC 30 may optionally emulate an IRRIGATION CONTROLLER, at least to the extent of accepting the same input control as an actual CONTROLLER and producing an output display that shows a display that would be upon an actual CONTROLLER's maintenance panel.



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The emulation further shows the valve actuations of the CONTROLLER and the times at which such occur.

The emulation is based on inputting data from KEYBOARD 33 into the PC 32 and then into appropriate data storage addresses of an actual irrigation control program that is resident within the PC. The time-of-day clock memory storage location of the irrigation control program is set. The irrigation control program is run under its previously mentioned assembler. Certain memory storage locations that represent results of execution of the irrigation control program, such as the message buffer and/or the valve states, are then inspected.

This series of operations can all be done piecemeal under the operating system of PC 30, normally under the MS-DOS operating system. However, the necessary interfacing is normally accomplished by use of a small executive program. The executive program leads the operator through those same programming steps which are used in setting up a controller on-site, but also employs the computer's screen graphics and printer capabilities in order to give the operator more information with less effort. The executive program also facilitates user archiving of program and system histories.

Custom graphics support can be provided for large users. In the case of a golf course, this would include course maps to allow the user to point to a subsystem he wants to work on rather than identifying it by code.

An electrical schematic of a preferred embodiment of MULTIPROGRAMMER 30 is discussed in conjunction with Figure 11.

### 2.3 Extension Maintenance Panel

A pictorial diagram of the extension maintenance panel in operational use is shown in Figure 4. An irrigation controller 1 that is normally modified so as to not have a control panel 20 (shown in Figure 1) is mounted at the top of a post 2. The post 2 may be ten feet or greater in height so as to protect the irrigation controller from inadvertent or

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intentional damage. A RIBBON cable 40 connection of digital accessory connector 14 (also shown in Figure 14) is extended interior to the hollow post 2 to JUNCTION BOX 41. The JUNCTION BOX 41 typically contains a coiled EXTENSION SERIAL CABLE, normally six feet in length. At the end of this cable an EXTENSION MAINTENANCE PANEL 42 is plugged.

The EXTENSION MAINTENANCE PANEL 42 replicates the same, or equivalent, display 21 and pushbutton switches 21-25 that are within the control panel 20 (shown in Figure 1). The maintainer-user 43 may realize equivalent control and exercise of the irrigation controller 1 through EXTENSION MAINTENANCE PANEL 42 as is normally realized through control panel 20.

#### 2.4 Radio-Linked Central Programming and Monitoring System™

A pictorial diagram of the radio-link central programming and monitoring system is shown in Figure 5. A radio-link module 50 mounts permanently below the controller 1 on the mounting pipe and serves as a transceiver for wireless communication between the controller and the radio-link CENTRAL STATION 51. This radio communication may be direct via path 52 or indirect via paths 53, 54 via a REMOTE RELAY RF UNIT 55.

The radio-link CENTRAL STATION 51 may be a MASTER or a SATELLITE. A MASTER CENTRAL STATION contains a personal computer (PC) 55 that drives a local CENTRAL STATION RF UNIT 56. Alternatively, a SATELLITE CENTRAL STATION 51 contains only a CENTRAL STATION RF UNIT 56 that communicates with the PC 55 of another, MASTER, CENTRAL STATION 51 via the RF UNIT 56 of that station and the TELEPHONE LINES 57. The TELEPHONE LINES 57 do not, of course, carry an RF signal. They can, however, carry that information which is either received or broadcast. RF to telephone conversion is implemented through a modem located in the RF unit.

A CENTRAL STATION 51 may be MOBILE, and mounted in a vehicle. In such a case the N irrigation controllers 1 may typically be programmed during drive-bys (insofar as the normal condition of the controller not to be energized is overcome).

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Typically a tuned RF circuit within the controller may be sufficiently energized by strong RF radiation so as to produce a voltage capable of bringing the irrigation controller 1, and its attached radio-link module 50, awake.

5           The radio-link CENTRAL STATION connects into same personal computer 55 that sends radio commands to the controller 1 via the radio link and receives information about the performance of the individual controllers and valves, along with data about soil moisture and other environmental  
10 parameters. The computer stores program information for all the controllers in the system in its memory and can operate the entire system remotely, via an emulated display panel identical to the on-site controllers. Sophisticated screen graphics and printer capabilities may be used to enhance operator  
15 convenience.

#### 2.5       Remote Test Command System

A pictorial diagram of a wireless remote test command system is shown in Figure 6. The remote test command system permits wireless remote "manual operation" of the valves and  
20 soil sensors of irrigation controller 1, in conjunction with an RF Test Adapter 60. This transceiver unit 60 is temporarily plugged into the controller 1 and receives "manual mode" commands from the hand-carried test commander 61. It also transmits soil sensor readings back to the hand-carried test  
25 commander 61. The portable hand-carried test commander 61 units are designed to be moved from controller to controller for installation, testing and maintenance purposes.

The hand-carried test commander 61 is a hand held transceiver carried by the installer or maintenance person.  
30 It is used for remote "manual mode" or test sequence operation of the valves and reading of soil sensors without having to return to the controller. This feature is especially useful in large systems. The hand-carried test commander 61 can save the installer/maintenance person considerable time, and miles  
35 per day of unnecessary walking, in testing for sprinkler

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performance, leaks, obstructions, and in checking soil sensor performance. The hand-carried test commander 61 will be used for a variety of applications such as activating watering zones only as long as necessary to cleanout the irrigation system, speeding up testing and inspections, and pinpointing cracks in pipe by turning water on briefly from the repair site, without flooding the entire area and for verifying proper operation after repairs are completed.

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3.0      Functional Description of the Preferred Embodiment of  
An Irrigation Controller in Accordance with the Present  
Invention

5      A preferred embodiment of an irrigation control system  
in accordance with the present invention is shown in Figure 2.  
An irrigation controller 1 (previously seen in Figure 1)  
operates under control of MICROPROCESSOR U2 (partial) executing  
programmed firmware that is resident in memories types ROM U4,  
RAM U5, and EE U9.      The MICROPROCESSOR U2 (partial)  
10      communicates with MANUALLY OPERABLE KEYS 22-25 (previously seen  
in Figure 1) for receipt of data and control. It interfaces  
with DISPLAY 21 (previously seen in Figure 1) for the display  
of questions, parameters, and help messages to a human  
user/programmer (as detailed in previous section 2.0).

15      The MICROPROCESSOR U2 (partial) of irrigation  
controller 1 optionally communicates externally through a  
SENSOR INTERFACE 26 of plugjack 16 (shown in Figure 1) to up  
to eight MOISTURE SENSING UNITS (optional) 27a-27h (shown in  
dashed line). This optional communication is the purpose of  
20      sensing soil moisture at up to eight locations. The  
MICROPROCESSOR U2 (partial) communicates through VALVE  
INTERFACE 28 of plugjack 13 (shown in Figure 1) to up to eight  
electromagnetically actuated CONTROL VALVES 29a-29h (shown in  
dashed lines). This communication is for the purpose of gating  
25      the flow of pressurized water from WATER SUPPLY 30 through a  
selected one of CONTROL VALVES 29a-29h at any one time to a  
corresponding one of WATERING HEADS 31a-31h (shown in dashed  
line).

30      The MICROPROCESSOR U2 (partial) may optionally  
communicate through plugjack 15 (shown in Figure 1) to OTHER  
DEVICES 32 (shown in phantom line) for purposes of receiving  
the download of firmware programs, parameters, and/or commands.  
This interface need not be enabled to operate the irrigation  
controller 1, which in preferred embodiment comes from the  
35      factory with that control program that is appendicized to this

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specification within its ROM memory U4 and EE memory U9, and which in the preferred embodiment may have all necessary parameters and control entered through MANUALLY OPERABLE KEYS 22-25. Indeed, if necessary firmware could be entered into controller 1 through it's MANUALLY OPERABLE KEYS 22-25. The digital interface to OTHER DEVICES 32 simply represents a less tedious way of communicating.

The preferred embodiment of the controller 1 normally derives all its power, and all power for MOISTURE SENSING UNITS 27a-27h and CONTROL VALUES 29a-29h, during quiescent operation both day and night from radiant light energy impingent upon RADIANT ENERGY CONVERTING UNIT (includes ASIC U1) that comprises each of PVM1, U1, and ASSOCIATED CIRCUITRY. "PVM" stands for photovoltaic module and "ASIC" stands for application specific integrated circuits. All "U" designations stand for integrated circuit chips that may be referenced in Figure 3 (to be discussed).

The preferred embodiment of controller 1 is powered during its operation to accept user programming not by the RADIANT ENERGY CONVERTING UNIT PVM1, U1, and ASSOCIATED circuitry but rather by electrical connection through plugjack 14 (shown in Figure 1) to the POWERKEY™ PLUGGABLE BATTERY ENERGY SOURCE 33. This SOURCE 33, normally not a part of irrigation controller 1 during its quiescent operation, is shown neither in shadow line for being optional, nor in dashed line for being related to the controller 1 of the present invention but not part thereof. Rather, the POWERKEY™ PLUGGABLE BATTERY ENERGY SOURCE is shown in solid line in order to illustrate that for the purposes of programming the controller in accordance with the present invention it must be present.

This required presence is because the SOURCE 33 supplies the greater power that the MICROPROCESSOR U2 (partial) needs to exit the predominantly somulent (inactive) state that it only intermittently and momentarily leaves to effect

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irrigation control in accordance with the schedules, and to assume a high duty cycle at operation. The SOURCE 33 also supplies the power requirements of MANUALLY OPERABLE KEYS 22-25 and of DISPLAY 21 during user programming. Although the energy storage within the RADIANT ENERGY CONVERTING UNIT might suffice to permit user programming, it is unwise to deplete this energy storage to an undetermined amount (dependent on the length and adeptness of user programming) -- especially at night when no energy recovery is possible and especially when the controller is programmed to immediately begin controlling irrigation cycles. Instead, the SOURCE 33 actually charges the energy storage means within the RADIANT ENERGY CONVERTING UNIT, and always leaves the controller 1 fully powered and ready to control irrigation of the end of a user programming sequence.

3.1 Hardware Description of the Preferred Embodiment of An Irrigation Controller in Accordance with the Present Invention

The schematic diagram of Figure 3a through Figure 3h, substantially a block diagram because the very substantial function of the circuit shown is contained in two Application Specific Integrated Circuits (ASICs) U1 (shown in Figure 4) and U2 (shown in Figure 5) -- shows the preferred embodiment of irrigation controller 1 (previously seen in Figures 1 and 2) in accordance with the present invention.

Commencing in Figures 3a and 3c, primary power is provided to the irrigation controller in accordance with the present invention by photovoltaic module PVM 1 or, alternatively, by a POWERKEY™ power source. The POWERKEY™ power source is a battery that is connected between terminals BAT + and BAT -. During programming of the irrigation controller 1 the POWERKEY™ power source (not shown) is always connected. Thereby the battery provides the considerable power necessary to energize the display LCD 1, and, importantly, operate the entire controller 1 at the high duty cycle necessary to conduct communications with the operator. The

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battery also serves to initially charge the capacitor power storage (both at a current limited rate) each time the POWERKEY™ battery power source is replugged to its receptacle 14 (shown in Figures 1 and 2). This insures that after each user interface communication the controller is always left in a fully charged condition.

During normal, quiescent, operation all low-power CMOS circuitry and the low-power valves are energized by energy stored in supercapacitors (SUPERCAPS) C1, C2. It is the function of first ASIC U1 to manage the voltage and power levels of the irrigation controller, and, most particularly, to control the charging of SUPERCAPS C1, C2 by PVM 1 and the POWERKEY™ power source. The SUPERCAPS C1, C2 will automatically be charged by connection of the POWERKEY™ power source. The ASIC U1 operates to control this charging through a constant current source implemented by transistors Q3, Q4 and resistor R2. This constant current source is controlled by a switching regulator implemented from transistor Q2, inductance L1, diode D4, and capacitors C3, C4, all under the control of ASIC U1. The switching regulator and constant current source act jointly to pass, during the presence of bright sunshine or of the POWERKEY™ power source, up to 63 milliamperes through steering diode D3 to charge SUPERCAPS C1, C2. The diodes D1, D2 prevent discharge of the charged SUPERCAPS C1, C2.

Continuing in Figure 2a, connections to the ASIC U1 that is used for power management and control include VDD 2. VDD 2 is the main +5 vdc power for the irrigation controller 1 and other components (such as CONTROL VALVES 29a-29h or MOISTURE SENSING UNITS 27a-27h both shown in Figure 2) to which it is attached in order to form an irrigation system. Signals BA and DX provide local control to the switching regulator and constant current source. The abbreviation NSL stands for system low voltage, NSVL stands for system very low voltage, NSH1 stands for the first shunt from the upper SUPERCAP, NSH2 stands for the second shunt from the lower SUPERCAP, and NBP



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produces a battery present control signal. The output PULSE is a real time clock interrupt of 30 microseconds duration occurring each 1/2 millisecond.

5 The logical control function of the irrigation controller 1 is substantially implemented by digital ASIC U2, shown extending across each of Figures 3b, 3d, 3f, and 3h. The main switch control inputs S1-S6 to ASIC U2, used for operator programming of the irrigation controller 1, are from corresponding switches S1-S6 shown in Figure 3a. The switches  
10 S1-S6 respectively implement the stop, unused, unused, help, no, and ok switch control inputs to ASIC U2. These switches S1-S6 are called the MANUALLY OPERABLE KEYS 22-25 in Figure 2.

Referring to Figures 3b and 3d, up to eight soil moisture sensors that are connectable to terminal block J3  
15 produce signals that are received into corresponding eight analog to digital converter channels, AD CH1 through AD CH8, of ASIC U2.

In a similar manner one side of each coil driver of up to eight valves that are hooked to the eight valve channels on  
20 terminal block J2 is internally connected within ASIC U2 as a signal input to one of the remaining eight analog to digital converter channels. Thus, ASIC U2 offers a total of 16 A/D channels, of which eight are internal and eight are external. The irrigation valve control, or drive, signals developed by  
25 ASIC U2 are brought to terminal block J2. This terminal block J2 is brought out to plugjack 13 shown in Figures 1 and 2.

Referencing Figures 2f and 2h the ASIC U2 operates on firmware instructions, and on parameters, that are stored within both read only memory ROM U4 and in random access memory  
30 RAM U5. The ASIC U2 addresses both such memories through ADDRESS DECODER U7. The irrigation controller 1 is generally versatily programmable, as well as parameterizable. Thus, many firmware instructions that ASIC U2 executes are present in RAM U5 and are loaded therein in accordance with user  
35 requirements. Other firmware instructions reside in ROM U4.

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Referencing Figure 3g, the irrigation controller 1 in accordance with the present invention connects to still another programmable memory other than RAM U5 (shown in Figure 3h). This is Electrically Erasable (EE) 1024 bit serial memory U9. This EE memory is particularly distinguished in that it will retain its informational contents in the total absence of power (unlike RAM U5). Yet it is alterable in its contents, unlike non-volatile ROM U4. The 1024 bit serial memory U9 permits the field programming of secret codes, vital set up information, and other information that is desirably user specified (unlike the factory-programmed informational contents of ROM U4), wherein this information will desirably not be lost during any interruption of power to the controller.

Circuits U6 (save for one unused spare gate shown in Figure 3c), U7, and U8 form a control interface of a standard type from ASIC U2 to the 1024 bit serial EE memory U9. In the address bus between the ASIC U2 and the control interface circuit U8, address line AD0 powers up, address line AD1 selects, and address line AD2 clocks serial data present on line AD3 into, 1024 bit memory U9. The single, serial, data output bit D0 of 1024 bit memory U9 is amplified in non-inverting element U10 and communicated to ASIC U2 as bit ADO upon its address bus.

The function of the circuits of irrigation controller 1, substantially contained in ASIC U1 and U2, to manage irrigation control will become increasingly clear upon the detailed discussion of such ASIC U1s and U2 in respective following sections 4 and 5.

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#### 4.0 Functional Description of the U1 ASIC Device

The block diagram of Figure 4 shows the overall architecture of the first, U1, Application Specific Integrated Circuit (ASIC) used within the preferred embodiment of the irrigation controller in accordance with the present invention. The detail function of ASIC U1 is essentially unimportant for the purposes of the present invention, and is included within this specification only for purposes of completeness. The photovoltaic module (PVM, shown in Figure 3a), SUPERCAPS C1 and C2 (shown in Figure 3a) and ASIC U1 (shown in Figure 3a) may be considered to simply be the implementation of a special form of a light-energized power supply. The general implementation of an a.c. or battery source power supply is, of course, routine in the electrical arts.

The U1 ASIC device is used to generate a 5 volt power supply using power from a photovoltaic module or battery. Power is stored by charging very large supercapacitors ("SUPERCAPS") to 10.8 volts. The stored energy is then used for operation during dark periods. Because the energy stored in the SUPERCAPS =  $1/2 CV_{cap}^2$ , the run time duration of the controller during conditions of darkness is greatly affected by how closely the maximum charge voltage can be brought to the maximum tolerable voltage for the SUPERCAP components. Therefore, to increase the dark run time, the "SUPERCAPS" are very carefully monitored, so that they may be charged to a maximum value without being over-charged.

The U1 ASIC device is designed to use minimal power while providing five (5) functions:

First, it monitors SUPERCAP voltages and shunts the charging current if they are over-charged. The monitoring holds this voltage to within +/- 1.75%.

Second, it provides a 5 volt +/-2.5%, 0-65 mA output voltage to power other electronics.

Third, it provides status signals indicating the condition of the power supply.

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Fourth, it provides a 2 kHz, 30 us pulse for use as a time base.

5 Fifth, it steps up a 9 volt battery to 17 volts to charge the SUPERCAPS and provide current during programming of other electronics. (Power consumption is less of a concern in this mode.)

10 Sampling capacitors are used to monitor the various capacitor and power supply voltages, allowing the use of only one comparator to conserve current. CrSi 100 k $\Omega$ / resistors are used to minimize analog currents.

The voltage reference is trimmed using on-chip metal fuses.

15 There are 3 potential 'most positive' voltages and two potential 'most negative' voltages, making substrate connections difficult. This is handled by using bipolar junction isolation that employs the isolated n- regions as separate CMOS substrates. This allows the CMOS circuitry to operate from several supplies, any one of which could be at the highest potential at different times.

20 The logic generally runs from VSS1 (0V) to VDD2 (0-5V), level shifting where required. Analog references run from VSS1 to VDD1 (0-11V). Switching regulator components run from VSS2 (-.7 to +5.5 V) to VBAT (0 to 15 V). The upper shunt transistor is connected to a voltage which can range from 0 to VDD1 +0.7V.

25 4.1 VREF1 Voltage Reference. The VREF1 circuit X4 is a voltage reference for monitoring supercaps, system low, and system very low. The circuit requires no op-amps, reducing offset error. NMOS transistors at collectors of non bandgap transistors are used to eliminate early voltage effects. The circuit has a buffered output which multiplies the bandgap voltage and is trimmed to 1.50 volts. This trimming is with on-chip metal fuses. The trim range is approximately 1.5 +/- 0.1 volts with minimum steps of 3 mV. An extra +/-1 LSB is provided in case original trim is incorrect. The circuit

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temperature coefficient is 60 ppm/°C typical, 150 ppm/°C worst case.

4.2 IBIAS & XTAL BIAS Bias Current Generator. The IBIAS & XTAL BIAS circuit X1 generates 20 nA bias currents for other cells, and 100nA bias (voltage) for xtal oscillator. It generates buffered 2 Vth voltage "VLOW" used to run the xtal oscillator and high-order dividers at low current. CrSi and p-resistors are combined to match TC of Vbe. The bias varies approximately +/- 28% over all parameters.

4.3 XTAL OSC & HIGH ORDER DIVIDERS. The XTAL & 2 kHz DIVIDERS circuit X2 generates a clock for capacitor switch sequencing. It uses a low current oscillator (CASC1 from TCJ) running from the second Vth supply voltage called VLOW. Internal trim capacitors are added to the crystal pins and are metal mask trimmable. Dividers to 2 kHz run from VLOW, then are level shifted to VSS1, VDD2 (0 to 5V). This avoids level shifting at 32 kHz, conserving current.

Circuit input PULSE receives a 2 kHz 30 microsecond pulse used for on and off chip timing. Circuit input NSTROBE receives a 2 kHz, 15 us negative pulse occurring 60 us after PULSE and is used for on chip timing. The level shifters use approx. 30 nA each at 2 kHz.

4.4 SAMPLING SWITCH DECODE. The SS DECODE circuit X3 is clocked by input PULSE. A one-shot is used to effectively generate a non-overlapped clock for the switch output signals. All switch signals are disabled (by inputs E and NE) for 0.6 to 4 us after each clock.

Switch sequencing samples the upper supercap, lower supercap, system low, and system very low in that order. Inputs NSC1, NSC2, NSSL, NSSVL define which voltage is being sampled. Each voltage is sampled once every 7.8 ms.

Input NCMP\_CLK is the comparator clock. Input NCMP\_ON powers down the comparator during unused periods.

4.5 SAMPLING CAP ARRAY & SWITCHES. The CAP ARRAY & SWITCHES circuit X5 contains sampling capacitors that are

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basically unit sizes. Due to the variety of voltages sampled, fractions of units are required. Poly etch tolerance can cause approximately 0.2% ratio error.

Inputs S1, S2, S3, S8 and S9 require signals level shifted above VSS2 (the normal logic level is VSS1, VDD2). Inputs S1, S2, S3, S8, S9 must have bodies tied to VSS1 & VDD1. All other switches may be tied to VSS1, VDD2. Note that this includes p-channel bodies, since they are isolated from the substrate in this process.

Sampling occurs such that the node OUT should remain at the reference voltage level if the sampled voltage is at its exact trip point. This avoids parasitic capacitance effects at this high-impedance node.

100 mV of hysteresis is added to the SL and SVL tests by switching between two slightly different capacitor values.

A simplified electrical schematic of the CAP ARRAY & SWITCHES circuit X5 illustrating its function is shown in Figure 5a. In operation,  $V_{OUT} = V_{REF}$  if  $V_{SAMPLE} \cdot C1 = V_{REF} \cdot C2$ .

4.6 SAMPLING COMPARATOR. The SCOMP circuit X7 compares output from the capacitor array to the reference voltage. It is inherently offset compensated. Its response time is less than 25us.

A simplified electrical schematic of the SCOMP circuit X7 illustrating its function is shown in Figure 5b. Phase 1 shorts the n-channel so that its gate voltage moves to the voltage where it carries exactly the current source current. The input capacitor is shorted to VREF and stores the difference between this gate voltage and VREF. Phase 2 opens the n-channel and connects the capacitor to the input voltage. If the input voltage is different from the reference, the gate is forced higher or lower, pulling the output of the current source down or allowing the current source to pull up.

4.7 COMPARATOR DATA LATCHES. The COMP DL circuit X11 stores the output of the comparator in the latch corresponding to the voltage being tested. It is clocked by input NSTROBE.

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4.8 WAIT TIMERS. The WT TIMER circuit X12 is used as a "timed hysteresis" when the SUPERCAP voltages are sampled.

When near the trip voltage, the capacitors will tend to be above the trip voltage when charging, and immediately  
5 fall below the trip voltage when the charging current is shunted away. This is due to approximately 7 $\Omega$  internal resistance in the SUPERCAPS.

The SUPERCAPS are sampled every 7.8 ms, and under the above conditions would alternate charging/discharging at a 50%  
10 duty cycle. A typical charge current of 20 mA would average 10 mA, while a typical load current is 12 mA continuous, resulting in a net energy loss. This would result in the capacitor charging to less than its maximum value by the internal I-R drop.

15 To avoid this situation, the comparator data latch is disabled for 3x7.8ms after it comes out of a shunt mode. This results in a 3:1 charge to shunt ratio, ensuring that the net charge current is positive.

4.9 SHUNT TRANSISTORS. The SHUNT TRANSISTORS X10 shunt up  
20 to 70 mA away from the SUPERCAP when the maximum voltage is exceeded. The SHUNT TRANSISTORS X10 have a resistance of approximately 3.5  $\Omega$ .

4.10 SWITCHING REGULATOR. The SWITCHING REGULATOR circuit  
25 X9 provides 17 volts from a 9 volt battery. The inductor shorting transistor of the circuit is off-chip (the IC is not required to handle the 17 volts).

Output NBP signals the VDD2, VSS1 logic when a battery is attached to the BAT, VSS2 terminals.

A simplified electrical schematic of a step-up DC-to-  
30 DC Converter circuit used in SWITCHING REGULATOR circuit X9 and illustrating its function is shown in Figure 5c. When switch S is closed the battery voltage is applied across the inductor L. Charging current flows through the inductor, building up a magnetic field, increasing as the switch is held closed.  
35 While the switch is closed, the diode D is reverse biased (open

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circuit) and current is supplied to the load by the capacitor C. Until the switch is opened the inductor current will increase linearly to a maximum value determined by the battery voltage, inductor value, and the amount of time the switch is held closed ( $I_{PEAK} = V_{BAT}/L \times T_{ON}$ ). When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a discharge current which flows through the inductor in the same direction as the charging current. Because there is no path for current to flow through the switch, the current must flow through the diode to supply the load and charge the output capacitor.

If the switch is opened and closed repeatedly, at a rate much greater than the time constant of the output RC, then a constant DC voltage will be produced at the output.

4.10.1 SWITCHING REGULATOR BIAS. The internal bias of SWITCHING REGULATOR circuit X9 is used only for biasing switching regulator components. The bias is provided by a Standard 5 uA bias cell type A54020. Its absolute value is not critical.

4.10.2 VREF2. The SWITCHING REGULATOR circuit X9 has an internal reference for monitoring switching regulator output voltage. The reference is provided by a standard cell reference type A53000 that is modified to use CrSi.

The reference circuit is chosen to keep non collectors at positive voltage. (Switching regulator can have voltages below the substrate voltage VSS1.)

The value and temperature coefficient of the circuit are not critical, and trim is not required.

4.10.3 RC OSC. The SWITCHING REGULATOR circuit X9 has an internal clock for switching the regulator at approx. 25 kHz. The clock is divided from 50 kHz to give a 50% duty cycle. It employs a standard cell reference type A55010 that is modified for CrSi. An approximate 150 k $\Omega$  external resistor is required.

4.10.4 SWITCHING REGULATOR COMPARATOR. The SWITCHING REGULATOR circuit X9 has a comparator that uses positive



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feedback for an improved response time of 3.5 us maximum.

4.11 VREG. The 5V REGULATOR circuit X6 provides a 5 volt +/- 2.5% regulated output for external electronics as well as VDD2 for internal logic. An external NPN is used to avoid thermal effects on the IC.

4.12 LOW VOLTAGE RESET. The LOW RESET circuit X8 resets the entire UI ASIC. The power supply can (under various light conditions) take minutes to hours for power up, which eliminates normal power-on-reset circuits. This circuit must ensure that all outputs are valid until the analog circuits are operational.

The output holds all latches in reset until the bias, reference, and regulator circuits are all running at levels acceptable for operation.

4.13 Preferred Technology for the U1 ASIC

The U1 ASIC is suitably implemented in BIPOLAR-CMOS technology available from several semiconductor foundaries. It is typically implemented in the BI-CMOS process of Micro-Rel Division of Medtronic, Inc., 2343 W. 10th Place, Tempe, Arizona 85281.

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## 5.0 FUNCTIONAL DESCRIPTION OF THE U2 ASIC DEVICE

The block diagram of Figure 6, consisting of Figure 6a through Figure 6f, shows the overall architecture of the second, U2, Application Specific Integrated Circuit (ASIC) used within the preferred embodiment of the irrigation controller in accordance with the present invention.

The U2 ASIC device is concerned with calculation, command, and control. It is primarily digital in operation, and may be considered to be a specialized microprocessor with substantial analog as well as digital I/O capabilities. The diagram of the U2 ASIC device shows the detailed interconnection of the various functional blocks.

### 5.1 U2 ASIC Device Architecture

5.1.1 Microprocessor. The central microprocessor Y31 of the U2 ASIC device is a NCR 65CX02 macrocell. It employs an 8-bit datapath structure controlled by an internal programmable logic array (PLA) using 8-bit instructions and having a 16-bit addressing capability. Importantly, all circuitry internal to the microprocessor is completely static and complementary so that the clock signal may be frozen and only leakage current will be consumed. It has a clock speed of 455 KHz and a 2.2 microsecond cycle time.

The microprocessor Y31 executes the instruction repertoire of commercially available microprocessor type 6502. The mnemonic codes for the instructions of this repertoire, such mnemonic codes, are commonly recognized mnemonics, and a complete description of the microprocessor type 6502 instruction repertoire, are contained, among numerous other places, in the book "6502 Assembly Language Programming" by Lance A. Leventhal, published in 1979 by Osborne/McGraw Hill, 630 Bancroft Way, Berkeley, California 94710. It will be recognized that, consonant with the modest computational requirements of an irrigation controller, the relatively simple 6502 microprocessor macrocell is not the sole type that could be employed, and that many microprocessors including types

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commonly incorporated in ASICs are suitable for use within the irrigation controller in accordance with the present invention.

The firmware instructions executed by micorprocessor Y31 occupy memory addresses in accordance with the following memory map table:

00-3F	I/O Parts
40-7FFF	RAM Memory U5 (shown in Figure 3h)
8000-FFFF	ROM Memory U4 (shown in Figure 3f)

The operand fields of the firmware instructions are interpretable in accordance with the following memory map table:

15	00	O	Microprocessor power off
	01	O	RTC counter clear
	02	O	A/D power, 1=on, 0=off
	03	O	A/D interface, 1=enable, 0=disable
20	04	O	LCD power, 1=on, 0=off
	05	O	LCD interface, 1=enable, 0=disable
	06	O	Valve select byte
			bits 0-2 - valve #, + side
			bits 3-5 - valve #, - side
25			bit 6 - polarity, 0=normal,
	1=reversed 07	O	Valve enable, 1=on, 0=off
	08	O	TIMER hi byte latch
	09	O	TIMER lo byte latch
	0A	O	TIMER control, 1=on, 0=off
30	0B	O	RTC, 1=10 seconds, 0=1 minute
	0C	O	Serial clock
	0D	O	TIMER load
	0E	O	Write serial data out
	0F	O	Serial output ready
35	10	I	RTC counter hi byte
	11	I	RTC counter lo byte
	12	I	Status register 1
			bit 0 - 0=external battery present
			bit 1 - 1=watchdog timeout
40			bit 2 - 0=system power low
			bit 3 - 0=system power very low
			bit 4 - 0=RTC pulse
			bit 5 - 1=battery low or caps charging
45			bit 6 - 1=serial data link present
			bit 7 - 0=serial data link ready
	13	I	Status register 2
			bit 0 - Switch 1, 1=pressed STOP
			bit 1 - Switch 2

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		bit 2 - Switch 3
		bit 3 - Switch 4 HELP
		bit 4 - Switch 5 NO
5		bit 5 - Switch 6 OK
		bit 6 -
		bit 7 - 0=A/D end of conversion
	14	I Read serial data in
	15	I Read A/D converter
	16	I Load serial shift register
10	17	I Clear input ready latch
	18	I LCD busy flag & address counter (RS=0)
		bit 7 - 1=busy
		O LCD instruction register (RS=0)
15	19	I LCD read data (RS=1)
		O LCD write data (RS=1)
	1A	O LCD contrast select (0-7)
	1B	O Clear watchdog timer
	1C	O Clock RTC counter
	1D	I/O EEPROM
20	1E	O Coil test drivers
	1F	O Sensor test drivers
	20	O Start A/D channel 0, sensor 1
	21	O Start A/D channel 1, sensor 2
	22	O Start A/D channel 2, sensor 3
25	23	O Start A/D channel 3, sensor 4
	24	O Start A/D channel 4, sensor 5
	25	O Start A/D channel 5, sensor 6
	26	O Start A/D channel 6, sensor 7
	27	O Start A/D channel 7, sensor 8
30	28	O Start A/D channel 8, valve 1
	29	O Start A/D channel 9, valve 2
	2A	O Start A/D channel 10, valve 3
	2B	O Start A/D channel 11, valve 4
	2C	O Start A/D channel 12, valve 5
35	2D	O Start A/D channel 13, valve 6
	2E	O Start A/D channel 14, valve 7
	2F	O Start A/D channel 15, valve 8
	30-3F	
	40-FF	Zero page variables, pointers, and tables
40	100-1FF	Stack
	200-3FF	Program variables
	8000	ROM start
	FFFA-FFFB	NMI vector
	FFFC-FFFD	RESET vector
45	FFFE-FFFF	IRQ vector

50     5.1.2     Drivers. The coil drivers Y20 work in pairs to supply relatively large bidirectional current pulses to operate

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electromagnetically actuated valves. Only one pair of coil drivers is active at a time, as specified by the contents of the data bus. Additionally, the output (coil) drivers have the capability to sink a regulated current for testing and programming purposes.

5.1.3 Timer. The timer Y26 consists of two 8-bit latches on the data bus and a 16-bit down counter which is clocked at 2 kHz. Loading of the counter and latches is under the control of the processor. When the counter reaches zero, a processor interrupt is generated.

5.1.4 ADC. The Analog-to-digital converter Y43 receives signals from external sensors and from the valves, a total of 16 channels in all, which are converted to digital information and placed on the data bus. The selection of the channel to be digitized is made on the basis of the contents of the address bus. The converted data is expressed as an eight-bit fraction. For the eight channels originating at the sensors and for the eight channels originating at the coils, this fraction is the ratio of the input voltage to the full power supply. All 16 ADC inputs may be pulled to ground through a poly resistor and an n-channel switch which together constitute a nominal 330 ohm resistance. The resistors associated with the eight channels originating at the sensors are enabled individually (as determined by the contents of the data bus) upon command of the processor. The performance specifications of the Analog-to-digital (A/D) Converter are as follows:

a. Resolution/Accuracy - 8 bits  $\pm$  one-half LSB for  $V_{IN} = 1(V_d)$

- 8 bits  $\pm$  one LSB for  $V_{IN} = 1/2 (V_d)$

b. Conversion Time -  $\frac{8}{f_{osc}} \times n$  where  $n = 8$  or  $9$  depending upon whether the conversion is full scale or half scale.

c. Operating Current - 3 mA maximum

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- d. Analog Reference - Digital Supply Voltage (Vd)
- e. Analog Inputs (Vin) - Each input voltage is ratio-metric with the digital supply voltage (Vd) where:

5 Vin for full scale =  $1/2(Vd)$  for A/D channels 1 through 8

Vin for full scale =  $1(Vd)$  for A/D channels 9 through 16

10 5.1.5 Clock/Calendar. This clock/calendar Y22 provides several timing functions. It generates a 2 second timing tick at 10 second or 1 minute intervals.

15 It keeps watch on the status of the programmer battery by generating a "Battery Low" status bit if either of two "Supercap Shunt" signals are absent for more than 64 second during programming activity.

It counts up to 65535 ticks while the processor is in a low voltage shutdown mode so as to provide calendar memory. The calendar contents may be placed on the data bus.

20 It maintains a 128 second dead-man timer which can generate a hardware reset if the processor fails.

5.1.6 Switch Register. The switch register Y2 acts as an interface between six external configuration switches and the data bus. An additional input is the end-of-conversion signal from the analog-to-digital converter.

25 5.1.7 Status Register. The status register Y3 makes the following internal flags available to the processor as data on the data bus: Battery Present, Dead-man timeout, System Low, System Very Low, Real Time Clock Tick, Battery Low, Serial Data Link Present, and External Ready.

30 5.1.8 Serial Data Link. The serial data link Y1 provides high speed synchronous two-way communication between the device and a remote data transceiver. Data is loaded or retrieved via the data bus under control of the processor. Transmission of serial data is also directly controlled by the processor.

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5.1.9 Ready. These circuits Y23 provide handshaking between the processor and an external device (such as a serial data link) through the status register and data bus.

5 5.1.10 Wakeup. The wakeup circuit Y27, upon stimulation by either the Serial Data Link Present or the clock/calendar time-  
tic or the Battery Present signals, starts the main system oscillator and then after a 500 microsecond delay, removes the system reset. Upon stimulation by the System Very Low signal or by the processor, the wakeup circuit immediately causes the  
10 system to be reset. The dead-man timeout signal will cause a 30 microsecond reset pulse to occur at two second intervals until the processor resets it.

5.1.11 Main Oscillator. The main oscillator Y25 uses an external capacitor and a charge-discharge scheme to produce a  
15 high-speed clock for the processor. This oscillator can be shut down to conserve power. It will restart immediately upon command. The frequency of oscillations is determined by the size of the external capacitor. The relationship between capacitor size and frequency, as well as the frequency  
20 stability over changes in operating environment, may be tailored in consideration of the operational environment within which the irrigation controller is used.

5.1.12 LCD Interface. The LCD interface Y29 consists of a latch on the data bus and the control circuitry needed to  
25 operate an external liquid crystal display and the DAC. The LCD interface can be configured to function as the 6502 Data I/O port. The interface is configured in this way only during a special test mode. Under processor control, a flip flop is set which alters the internal logic paths so that the LCD bus  
30 will be configured as a 6502 Data I/O port. This special test feature allows the 6502 to be tested independently of the peripheral logic.

5.1.13 DAC. The four bit digital-to-analog converter Y32 provides a voltage, as specified by the contents of the data  
35 bus, through the LCD interface for contrast control of the

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external liquid crystal display.

The performance specification of the DAC are as follows:

- a. Resolution: 4 bits
- b. Accuracy :  $\pm 1/2$  LSB for all voltage steps
- c.  $V_{out} = n(0.147)$  where  $0 \leq n \leq 15$
- d.  $I_o$  (min) = 500  $\mu$ A sink for  $V_{out} = 0V \pm 50$  mV
- e.  $V_o$  (max) =  $\pm 50$  mV for  $I_o = 500$   $\mu$ A for the DAC setting  $D_3 = D_2 = D_1 = D_0 = 0$

10 5.1.14 Address Decoding. The address decoder circuit Y38 uniquely maps all internal functions into page zero of the processor's memory space. The decoder produces timing and control signals for these internal circuits as well as for reading and writing of external memory.

15 5.1.15 Power Switching. The power switch circuit Y28 controls the power for the external ROM and display as well as the internal analog functions in order to conserve power and to permit the irrigation controller to enter a "sleep" mode.

20 5.1.16 Resistor Control. The resistor control circuit U42 permits reconfiguration of the sensor and coil interfaces to enable communication upon each of the A/D channel lines so that integrity of both valve coils and moisture elements may be self-tested. This is accomplished by selectively switching a low value resistor between the channel signal line and ground.

25 5.2 U2 ASIC Input/Output Description

30 5.2.1 CD0 - CD15 - Coil Driver Outputs. These pins operate in pairs, one pair at a time, when driving the coils of the electromagnetically actuated valves. One pin of the pair goes high while the other goes low in order to provide bidirectional current. Inactive coil driver pairs assume a high impedance state. When the coil is deenergized the driver circuitry must absorb the energy of the collapsing field. CD8 - CD15 also function as analog inputs to the ADC. These pins have the additional capability of sinking a regulated current for  
35 testing and programming purposes.



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5.2.2 ADC0 - ADC15 Analog Inputs to the ADC. These pins provide information from the coils and sensors whose integrity the processor must evaluate. ADC8 - ADC15 are shared with the 8 valve lines CD8 - CD15. ADC0 - ADC7 are shared with the 8 sensor lines. All these 166 lines have the capability of sinking a regulated current for testing purposes.

5.2.3 SL - System Low. An active low input indicates that the condition of the power supply is such that further operation will soon be impossible. The processor, upon receiving this signal, will immediately turn off all valves in anticipation of approaching shutdown.

5.2.4 SVL - System Very Low. An active low signal indicates that the condition of the power supply is such that further operation is impossible. Upon receiving this signal the processor will immediately go into hibernation. After approximately 100 milliseconds, a hardware system reset will occur independently of the processor.

5.2.5 SH0, SH1 - Supercap Shunt Signals. If either of these signals persists in the high state for longer than 64 seconds, a Battery Low status will be generated.

5.2.6 BPR - Battery Present. An active low signal indicates that a battery is connected to the power supply so that the processor may run continuously.

5.2.7 S1 - S6 - Switch Inputs. Active high inputs with internal pulldowns go directly to the switch register.

5.2.8 A0 - A14 - Address Outputs. The external RAM and ROM are addressed by these pins. A0 - A7 in conjunction with ALE also functions as D0 - D7.

5.2.9 D0 - D7 - Bidirectional Data Bus. The external RAM and ROM use these lines for transferring data to and from the device. The lower address bits are multiplexed with the data on these lines in conjunction with the ALE signal.

5.2.10 ALE - Address Latch Enable. When this signal is high, data transfers may take place on the D0 - D7 pins. When this signal is low, these same pins are used as A0 - A7 outputs.

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5.2.11 RDYIN - Ready Input. This signal appears as one of the bits of the status register. RDYIN provides handshaking protocol from a distant serial data link. A low-to-high transition of this signal sets the Serial Data Link Present status bit low. The signal is provided with an internal pulldown.

5.2.12 RDYOUT - Ready Output. This signal passes the contents of data bus bit zero out of the device under control of the processor to provide handshaking protocol to a distant serial data link.

5.2.13 CEROM - ROM Chip Enable. This signal is used to enable the outputs of the external ROM onto the D0 - D7 pins.

5.2.14 LCD0 - LCD7 - Liquid Crystal Data. These bidirectional signals transfer data to and from the external liquid crystal display. They are provided with internal pulldowns.

5.2.15 LCDEN - LCD Enable. This output signal enables the external liquid crystal display. This output signal can be made to exhibit high impedance with an internal pulldown.

5.2.16 LCDRS - LCD Register Select. This output signal informs the external LCD module that either data or command appears on the data inputs. This output signal can be made high impedance with an internal pulldown.

5.2.17 LCDRD - LCD Read. This output signal controls the direction of data flow to or from the external liquid crystal display. This output signal can be made to exhibit high impedance with an internal pulldown.

5.2.18 VLCD - Analog Output From the DAC to the External Liquid Crystal Display. This analog output signal is used to control the display contrast.

5.2.19 VL - Switched Power to the External Liquid Crystal Display. When this signal is switched on it provides current from the device power input VDD. When it is switched off, it sinks current into the device power return VSS.

5.2.20 VA - Switched Power to the External Sensors. When this signal is switched on, it provides current from the device

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power input VDD. When it is switched off, it sinks current into the device power return VSS.

5.2.21 VP - Switched Power to the External ROM. When this signal is switched on, it provides current from the device power input VDD. When it is switched off, it sinks current

5.2.22 Serial Clock - Clock Input/Output for Serial Data Transfer. When driven by the device for outward data transmission, this signal alternatively assumes a low impedance high state and a low impedance low state. If the low state persists for more than 20 to 40 nanoseconds then the signal remains at a high impedance with an internal pulldown. In this last state, the pin may be driven by an external source for inward data transfer (reception). The clocks generated by this pin may have a rate of up to 32,000 Hertz. This pin may be loaded with up to 300 picofarads capacitance.

5.2.23 Serial Data - Data Input/Output for Serial Data Transfer. When driven by the device for outward data transmission, this signal assumes a low impedance state whenever the Serial Clock is high, and then, if the clock low state persists for more than 20 to 40 nanoseconds, a high impedance with an internal pulldown. In this last state, the pin may be driven by an external source for inward data transfer (reception). The data generated by this pin may have a rate of up to 32,000 bits per second. This pin may be loaded with up to 300 picofarads.

5.2.24 C01, C02 - Capacitor Connections. Provides a connection for a capacitor whose value determines the frequency of the Main Oscillator.

5.2.25 READ (WRITENOT) - R/W Signal From the Processor. Indicates whether a memory read or memory write cycle is in progress.

5.2.26 PH12 - Processor Clock. This signal is high during the active portion of the processor's operation. When low, the processor is precharging its internal busses. This signal must

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logically combine with Read and the appropriate address decode to create the control signals to apply to external memory.

5.2.27 CSE2 - EEPROM Chip Select. This signal is used in conjunction with READ and PH12 for external EEPROM operations.

5 5.2.28 RSTB - Processor Reset. This active-low signal indicates that the processor is shut down and may be used to initialize external circuitry to the correct state for processor startup.

10 5.2.29 PAGE0 - Page Zero. This pin goes high when the address bus is in address area 0040H through 7FFFH inclusive.

5.2.30 VDD - Device positive supply.

5.2.31 VSS - Device negative supply.

15 5.2.32 CK - Real-Time Clock Input for Clock Calendar Timer. The frequency is nominally 2Khz with a 30u second high-going pulse.

5.2.33 SPSEL. When SPSEL = 1, the chip requires a 32Khz time base on the CK input. When SPSEL = 0, the chip requires a 2Khz time base on the CK input.

### 5.3 ASIC U2 Power Supply Requirements

20	<u>Parameter</u>	<u>Symbol</u>	<u>Min</u>	<u>Max</u>	<u>Units</u>
	Power supply	VDD A	4.5	5.5	V
	All circuitry active				
	-----				
	Power Supply	VDD B	2.00	5.5	V
25	Real time clock, interrupt, and battery low detection circuitry operative. All other circuits are at a static, defined logic level (therefore, not being clocked).				
	-----				
	Active Supply Current	Ia		6.0	mA
30	VDD = 5.5v, 2Khz Real time clock running, main oscillator running, processor, ADC, LCD interface logic running (only), DAC running, coil drivers in high-impedance state, external interface circuitry to EEPROM, ROM and RAM is active, however, the active current of the EEPROM, ROM and RAM is not included.				

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Quiescent Supply Current  $I_q$  1.5 uA

VDD = 5.5v, Real time clock running, main oscillator stopped, processor stopped, coil drivers in high-impedance state, ADC, LCD, DAC are all powered off. External EEPROM and ROM are powered off. External RAM is at a static, defined logic level (therefore, not being clocked). The quiescent current of the RAM is not included in  $I_q$ .

## 5.4 ASIC U2 Signal Pin Requirements

Unless otherwise stated, the following characteristics apply over the applicable operating power supply range as specified above. All pins are protected against electrostatic discharge.

	<u>Parameter</u>	<u>Symbol</u>	<u>Min</u>	<u>Max</u>	<u>Unit</u>
15	Capacitance of Inputs	Ci		10	pF
	Capacitance of Outputs	Co		10	pF
	Capacitance of Tristate	Ct		10	pF
	Input Leakage Current	Iil	-1	+1	uA
20	Tristate Leakage Current	Itl	-1	+1	uA
	Passive Pulldown Current	Ipd	-1	-30	uA
	(@ Vih = VDD)				
	Active Pulldown Current	Irp	-4	-12	mA
	(@ Vi = 2.5v)				

VA, VL, VP

	<u>Parameter</u>	<u>Symbol</u>	<u>Min</u>	<u>Max</u>	<u>Unit</u>
	Output High Voltage	Voh	VDD-0.3	VDD+0.3	V
	Output Low Voltage	Vol	-0.3	+0.4	V
30	Output High Current (@ Voh = VDD-0.3V)	Ioh	-6.0		mA
	Output Low Current	Iol	6.0		mA

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VLCD

	<u>Parameter</u>	<u>Symbol</u>	<u>Min</u>	<u>Max</u>	<u>Unit</u>
	Output Voltage Range	Volcd	0.0	2.2	V
5	Output Current (@ Vol = 0.05V)	Ioled	+0.5		mA

Coil Driver Pins

	<u>Parameter</u>	<u>Symbol</u>	<u>Min</u>	<u>Max</u>	<u>Unit</u>
	Input Voltage Range	See ADC8 - ADC15 below			
10	Output Pair Drop (@ I = 45mA, Vdd = 4.5v)	Vdr	0.0	1.0	V

ADC0 - ADC15

	<u>Parameter</u>	<u>Symbol</u>	<u>Min</u>	<u>Max</u>	<u>Unit</u>
15	Input resistance	Rin	10Meg		Ohm
	Input Voltage Range	Vina	-0.0	VDD	V

C01, C02

	<u>Parameter</u>	<u>Symbol</u>	<u>Min</u>	<u>Max</u>	<u>Unit</u>
20	Output High Voltage	Voh	0.5	VDD+0.3	V
	Output Low Voltage	Vol	-0.3	0.4	V
	Output High Current (@ Voh = 2.5V)	Ioh	-4.0	-12.0	mA
	Output Low Current (@ Vol = 0.4V)	Iol	4.0		mA
25					

All Other Pins

	<u>Parameter</u>	<u>Symbol</u>	<u>Min</u>	<u>Max</u>	<u>Unit</u>
	Input High Voltage	Vih	2.0	VDD+0.3	V
30	Input Low Voltage	Vil	-0.3	0.8	V
	Output High Voltage	Voh	VDD-0.5	VDD+0.3	V
	Output Low Voltage	Vol	-0.3	+0.4	V
	Output High Current (@ Voh - VDD-0.5V)	Ioh	-2.0		mA
35					

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Output Low Current                      I<sub>ol</sub>                      4.0                      mA  
 (@ V<sub>ol</sub> = 4.0V)

## 5.5      ASIC U2 Mechanical Characteristics

5      5.5.1      Package Requirements. The device is packaged in an 84-pin plastic leaded chip carrier. The package life exceeds 20 years.

10      5.5.2      Environmental Requirements. The limits below represent the environmental limits to which the device will ordinarily be subjected.

	<u>Rating</u>	<u>Value</u>	<u>Unit</u>
	Storage Temperature	-40 to +85	deg C
	Operating Temperature	-10 to +70	deg C
15	Lead Temperature (4 min soldering)	250	deg C
	Humidity	85/85	deg C/percents

20      5.6      Preferred Technology for Implementation of the U2 ASIC  
 The preferred embodiment of ASIC U2 is preferably implemented in the CMOS technology of NCR Corporation, Dayton, Ohio. This technology, and the design rules and standard cells therein, is discussed in the "NCR ASIC Data Book" for January 1987. The equivalent technologies of other manufacturers will  
 25      be realized to be equally suitable. It will be understood that the irrigation system of Figure 2 could also be implemented using standard integrated circuit and microprocessor components in combination with a control program corresponding to that of attachment A. Such a system could be used alternately to  
 30      implement the present method.

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#### 6.0 The Preferred Embodiment of the Multiprogrammer Unit

A block diagram of the preferred embodiment of the Multiprogrammer usable in the distributed multiple irrigation controller control management system of the present invention is shown in Figure 11. A schematic diagram of the same Multiprogrammer unit is shown in Figures 12, consisting of Figures 12a through 12c.

As is visible from both figures, the Multiprogrammer unit 30 (previously seen in Figure 3) is based on both the ANALOG ASIC U1 and the DIGITAL ASIC U2 previously seen within the irrigation controller of Figure 7, and respectively individually illustrated in Figures 8 and 10. The ANALOG ASIC U1 connects to a BATTERY 70 which may be, but need not be, configured the same as the POWERKEY™ pluggable battery energy source. The ANALOG ASIC U1 operates to provide 5 volt dc regulated power to remaining components of the Multiprogrammer unit 30 from the power provided by the BATTERY 70. The BATTERY 70 connects through jack J1 terminals 2 and 7 to provide power to the irrigation controller when the multiprogrammer unit 30 is plugged thereto. The DIGITAL ASIC U2, containing the microprocessor type 6502, operates on a stored firmware program contained with ROM 71. This program causes the DIGITAL ASIC U2 to communicate through standard universal serial interface UART 72 type 65C51 across an interface I/F type RS232 73. This serial interface connects to a like serial interface port of a computer, particularly the personal computer PC 32 shown in Figure 3.

The communication path through the RS232 I/F 73 permits the DIGITAL ASIC U2 to receive information that is subsequently stored within RAM 74. The RAM 74 is nominally 512 K by 8 bits in size, and is of type 622S6. At this size it is capable of holding 64 complete programs as are uploaded to those IRRIGATION CONTROLLERS 1 (shown in Figure 3) to which the Multiprogrammer unit 30 at times connects.



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The detailed block diagram shown in Figure 12 shows the particular wired interconnection of the functional elements block diagrammed in Figure 11, and more particularly shows the interface between the Multiprogrammer unit 30 and the  
5 irrigation controller 1.

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7.0 Variations and Adaptations of the Invention

Although the present invention has been taught in the context of electrical circuits that are fairly sophisticated for employing both a predominantly analog ASIC (ASIC UI) and a predominantly digital ASIC (ASIC U2), it should be understood that the functionality of the preferred embodiment of an irrigation controller in accordance with the present invention is readily realizable by diverse alternative designs. In particular, the core microprocessor of the preferred embodiment of the invention is 100% compatible with industry standard type 6502. All firmware appended to this specification will execute on a 6502 microprocessor, and is readily convertible to alternative microinstruction repertoires executing on alternative microprocessors. The circuits by which data is manually input to the microprocessor and displayed, and the control of irrigation valves, are, in the preferred embodiment of the invention, powered and sequenced to states of activity in a highly unique manner. Nonetheless, it will be recognized that alternative power and sequencing of these circuits, particularly as consume higher power and/or operate at higher or continuous duty cycles, are readily realizable by a practitioner of the electrical design arts. Accordingly, the present invention should be considered in terms of the functions that it performs, and not solely in terms of any particular embodiment for realizing these functions.

In accordance with these and other aspects and attributes of the present invention, the invention should be determined by the scope of the following claims, only, and not solely in accordance with those particular embodiments within which the invention has been taught.

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## CLAIMS

What is Claimed is:

1. A method of programming an irrigation controller comprising:

generating a program, executable by an irrigation controller in order to control irrigation, off-line in a computer and not within any irrigation controller that will in fact execute the program to control irrigation;  
downloading the generated program from the computer into a transportable memory device capable of holding the generated program;

transporting the transportable memory device to an irrigation controller;

communicatively connecting the transportable memory device with the irrigation controller through a communication connection;

uploading the program from the transportable memory device into the irrigation controller through the communication connection;

communicatively disconnecting the transportable memory device from the irrigation controller, leaving the irrigation controller programmed with the generated program;  
and

repeating the generating, the downloading, the transporting, the communicatively connecting, and the communicatively disconnecting until a plurality of irrigation programs are loaded into an associated plurality of irrigation controllers;

wherein each of the plurality of programs is subsequently executable by that one of the plurality of irrigation controllers into which each program is loaded in order to effect the control of irrigation.

2. The method of claim 1 expanded for the programming of plurality of irrigation controllers that are

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interrelated in their performance of an irrigation function within a single irrigation system, the expanded method according to claim 1

wherein the off-line generating is of a plurality of different irrigation programs each executable by a corresponding one of a plurality of interrelated irrigation controllers, the plurality of programs being suitably interrelated so as to permit, upon their execution by the plurality of interrelated irrigation controllers, coordinated irrigation within an irrigation system;

wherein the downloading is of the plurality of generated irrigation programs into a transportable memory device capable of simultaneously holding each such program;

wherein the transporting is of the plurality of irrigation programs simultaneously;

wherein the communicatively connecting is to each of the plurality of irrigation controllers in turn;

wherein the uploading is of a one of the plurality of irrigation programs into an associated one of the plurality of irrigation controllers; and

wherein the plurality of programs are subsequently executable by the associated plurality of irrigation controllers to effect the coordinated control of irrigation within a single irrigation system.

3. The expanded plural irrigation controller programming method according to claim 2

wherein the uploading of each one of the plurality of irrigation programs into its associated one of the plurality of irrigation controllers is automatic, and without human intervention other than the communicatively connecting.

4. The expanded plural irrigation controller programming method according to claim 2 that, while at least one of the plurality of irrigation controllers is communicatively connected to the transportable memory

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device, further comprises:

loading information from a communicatively connected irrigation controller into the transportable memory device.

5. The expanded plural irrigation controller programming method according to claim 4

wherein the loading is of historical data on the irrigation control effected by that irrigation controller that is communicatively connected.

6. The expanded plural irrigation controller programming method according to claim 4

wherein the loading is of the program that was within the communicatively connected irrigation controller prior to the uploading.

7. The irrigation controller programming method according to claim 1

wherein the off-line generating is in a computer system emulating an actual irrigation controller.

8. The irrigation controller programming method according to claim 1

wherein the downloading of the generated program is into the memory of a transportable memory device having a memory; and

wherein the uploading of the program is from the memory of the transportable memory device.

9. The irrigation controller programming method according to 1 that while the irrigation controller is communicatively interconnected to the transportable memory device further comprises:

loading information from the communicatively connected irrigation controller into the transportable memory device.

10. The irrigation controller programming method according to claim 1 that, while the irrigation controller

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is communicatively interconnected to the transportable memory device, further comprises:

connecting power from the transportable memory device to the irrigation controller through a power connection; and

supplying power from the transportable memory device to the irrigation controller via the power connection for the irrigation controller's uploading of the program.

11. The irrigation controller programming method according to claim 1 that, at other times than the transportable device is communicatively connected to the irrigation controller, further comprises:

connecting to the irrigation controller at it's same physical port that is otherwise and at other times used for communicatively connecting to the transportable device another device suitable to exercise the controller; and

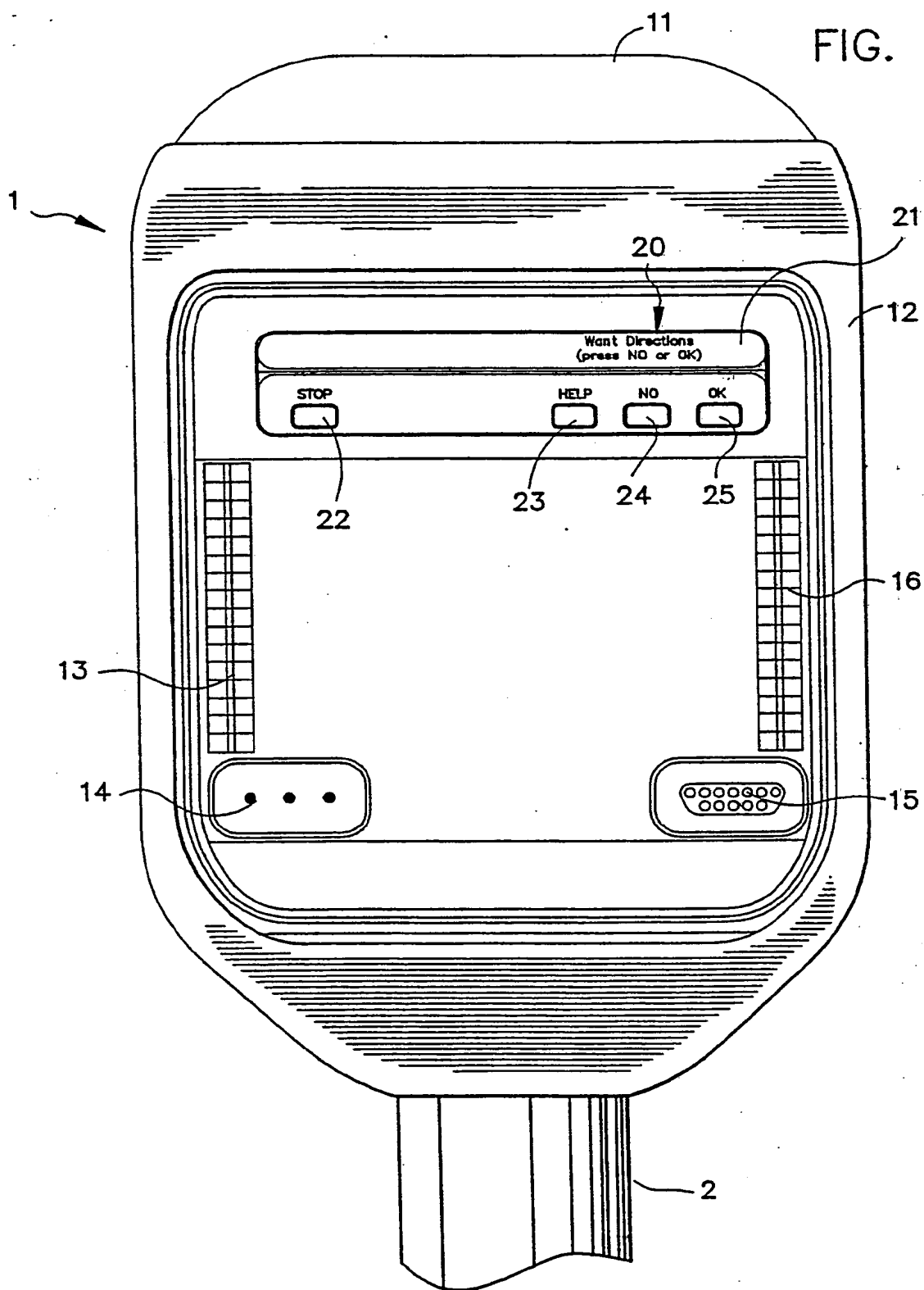
exercising the irrigation controller by a connected controller exercise device.

12. The irrigation controller programming method according to claim 11, wherein the exercising comprises:

causing the irrigation controller to turn on an irrigation valve that is connected to, and controlled by, the irrigation controller.

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FIG. 1



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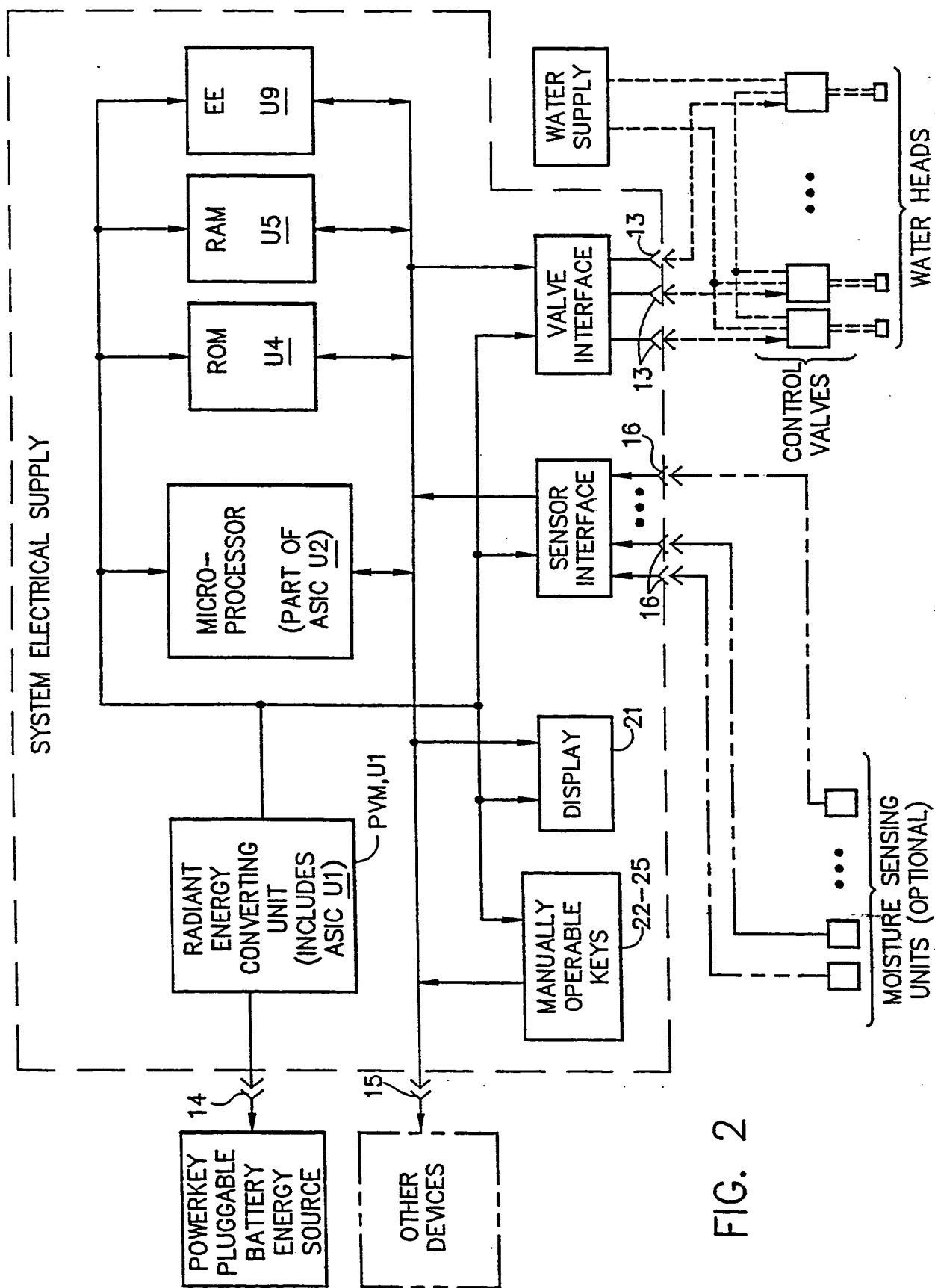


FIG. 2



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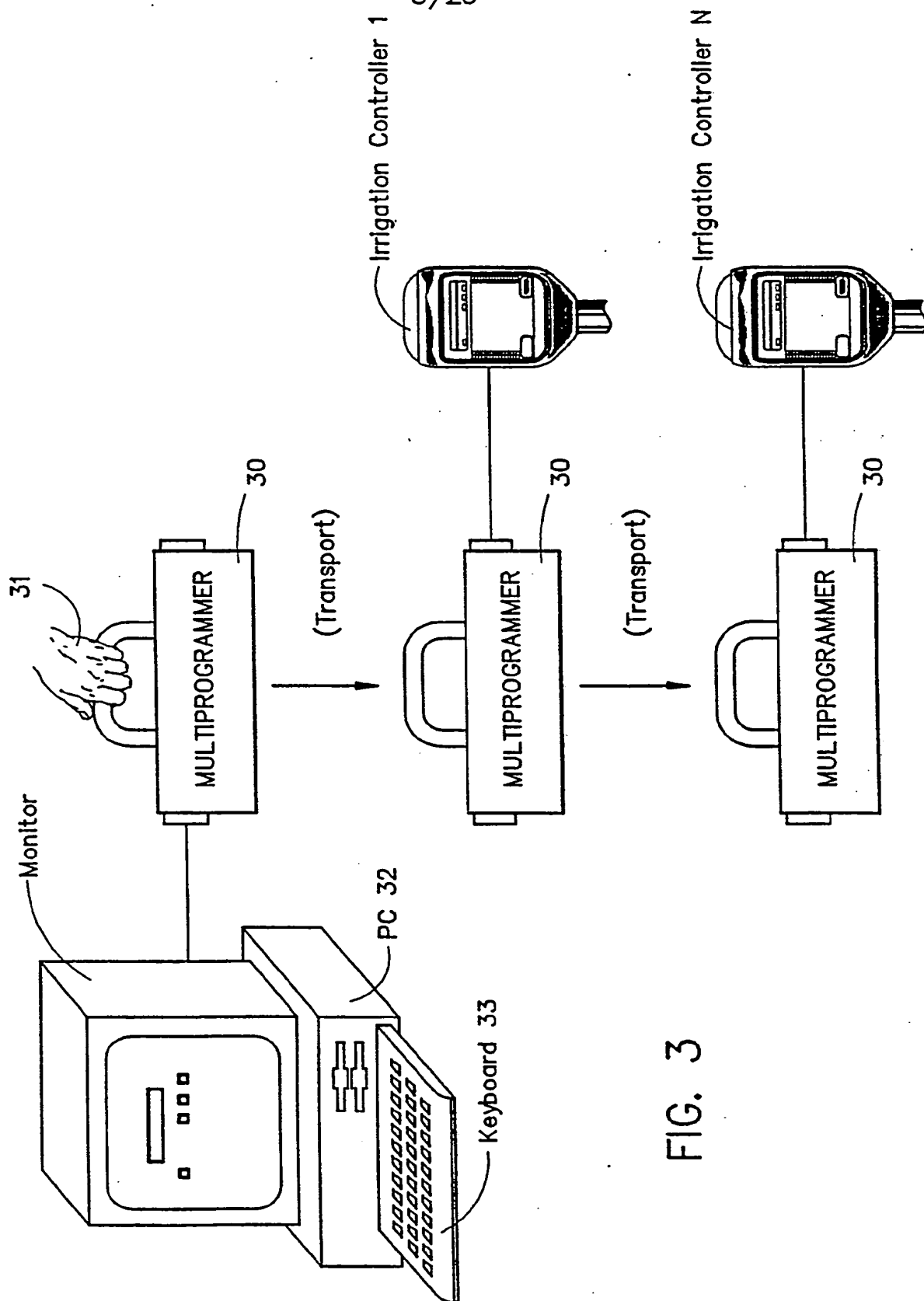
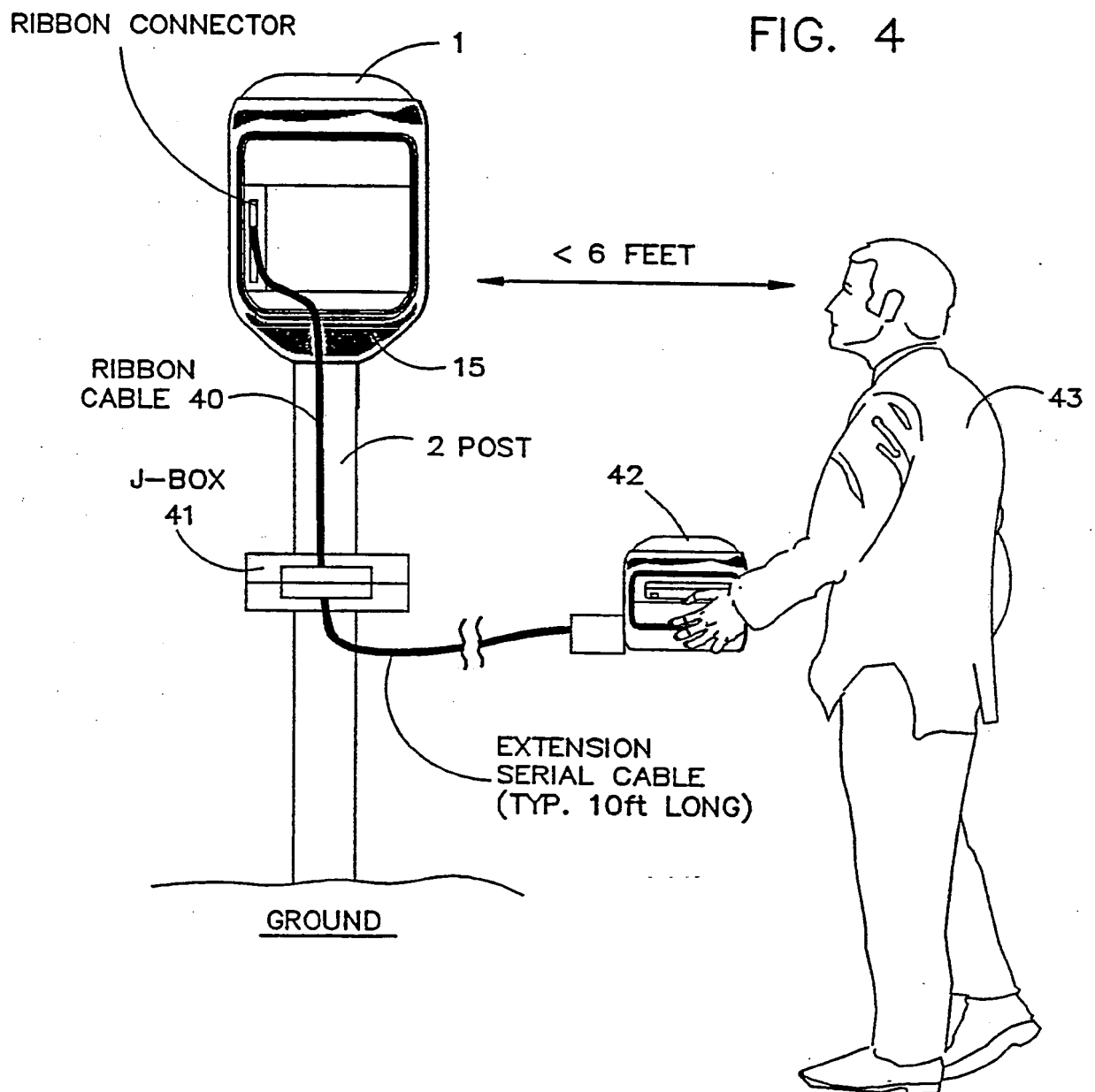
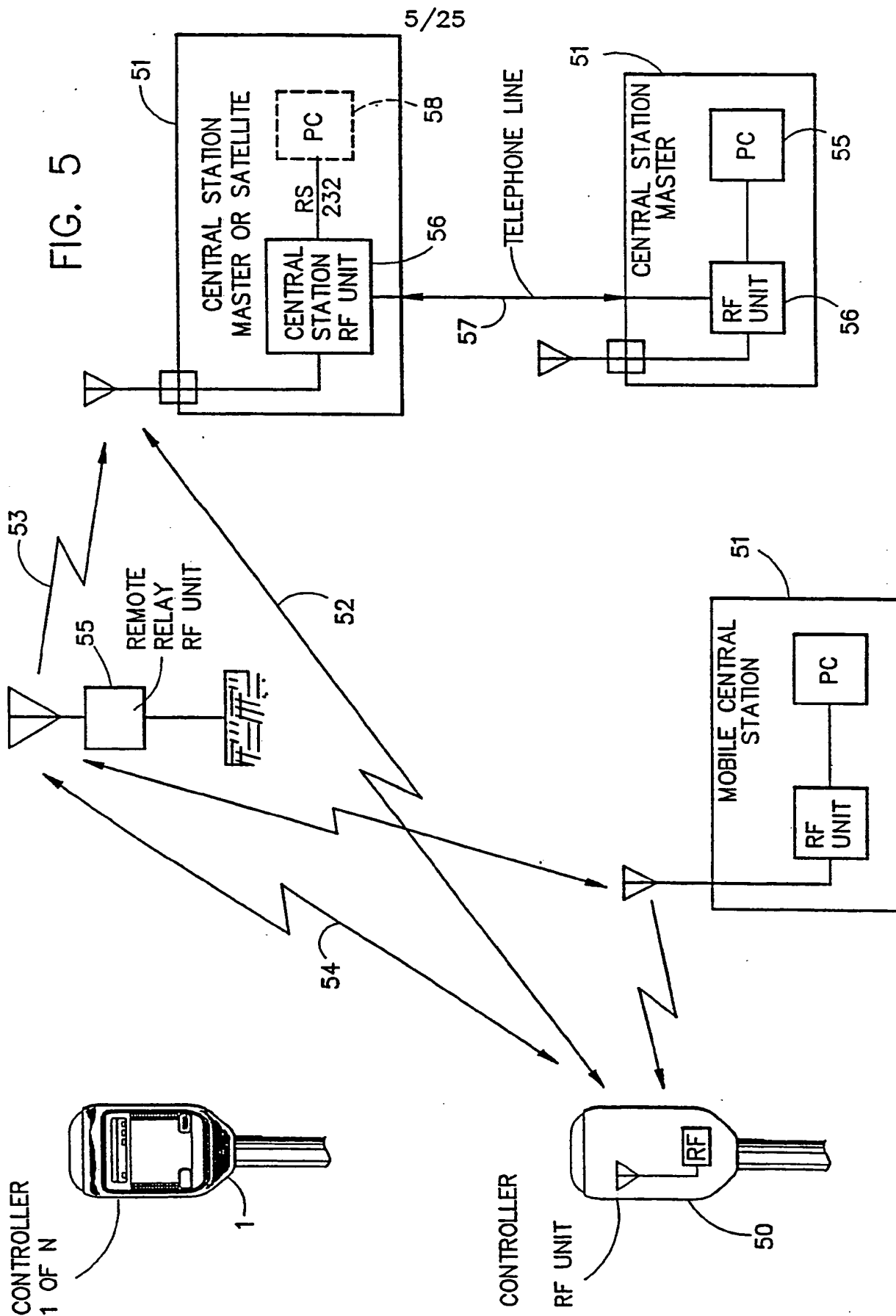


FIG. 3

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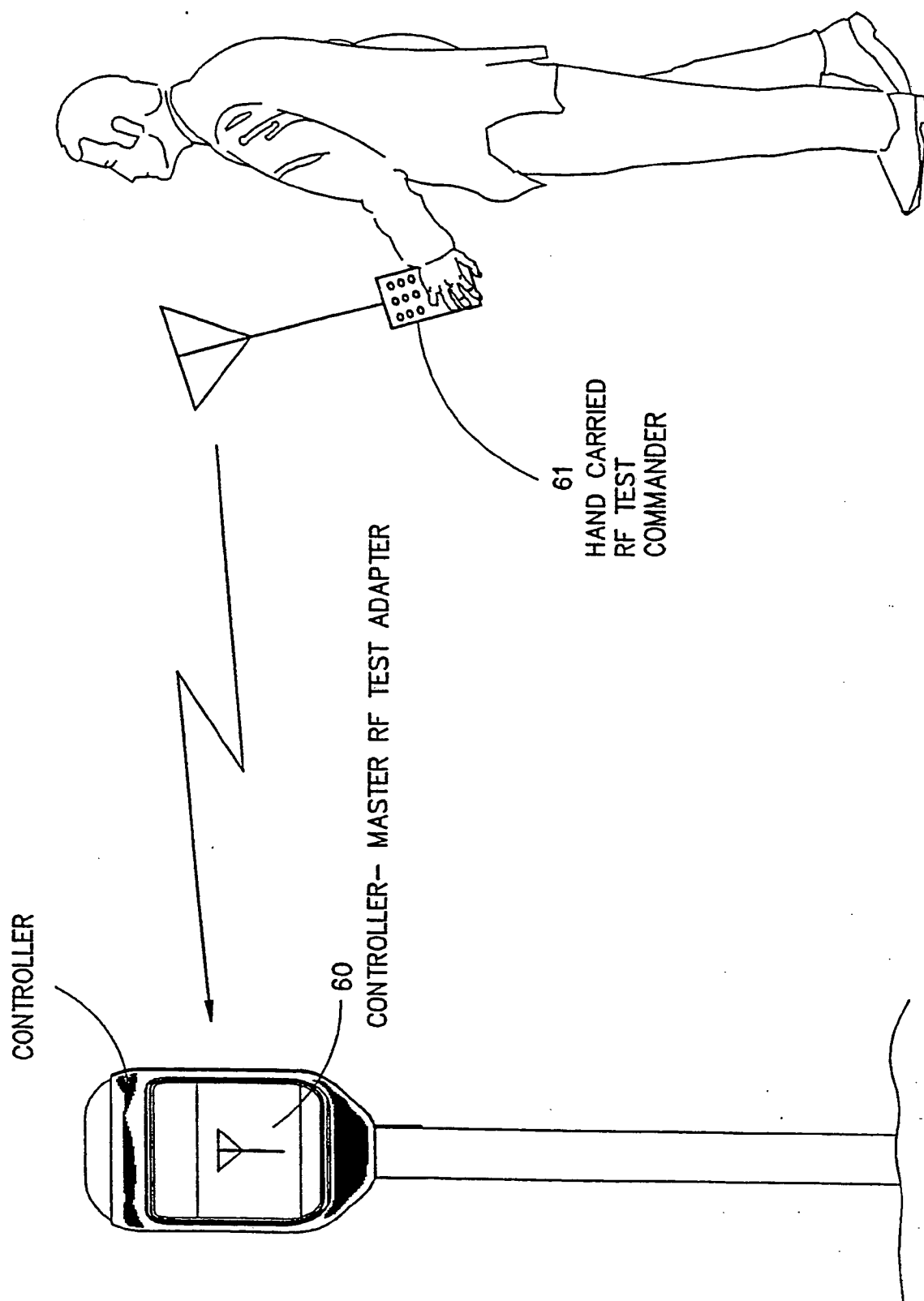
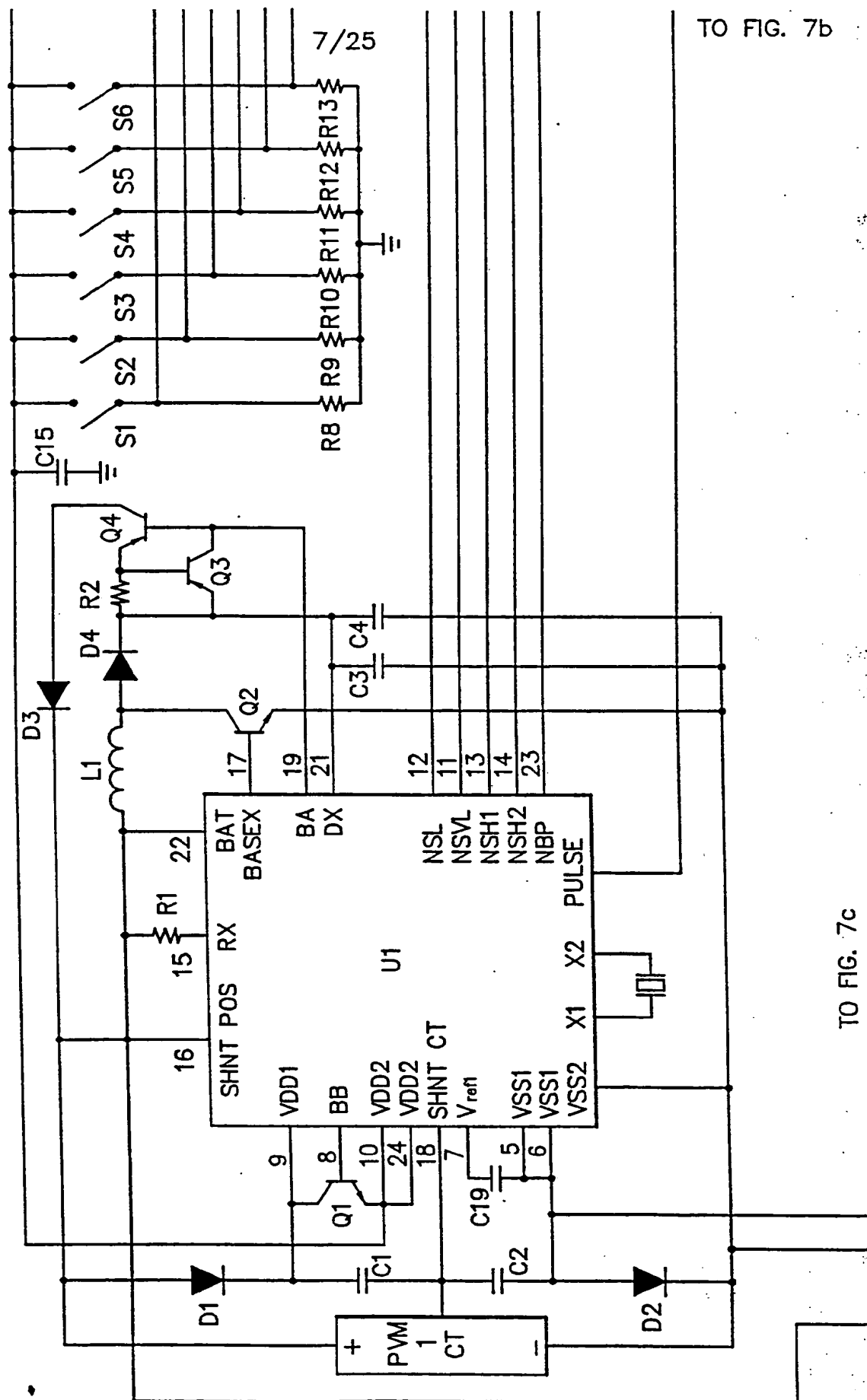


FIG. 6

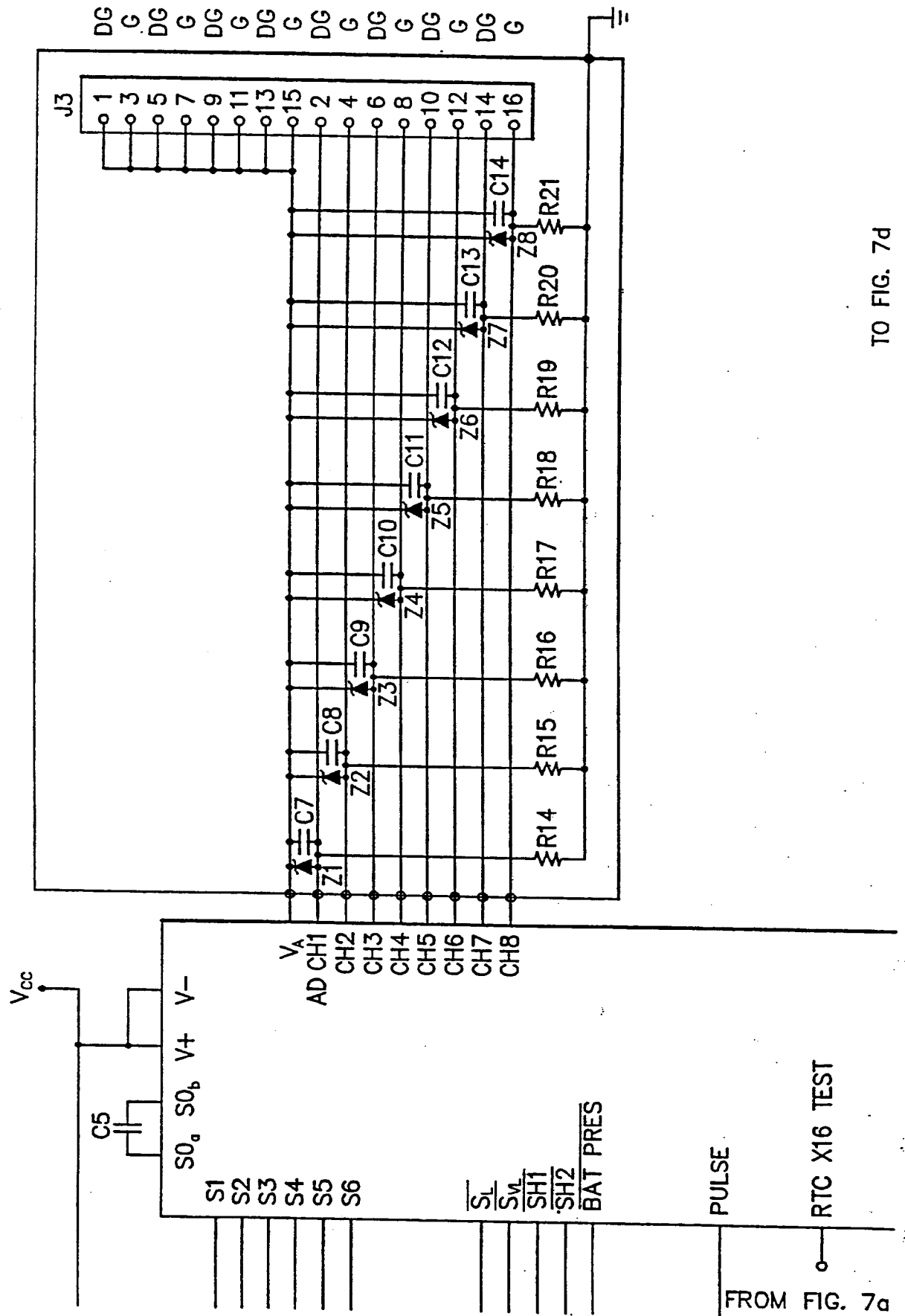
FIG. 7a



TO FIG. 7c

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FIG. 7b

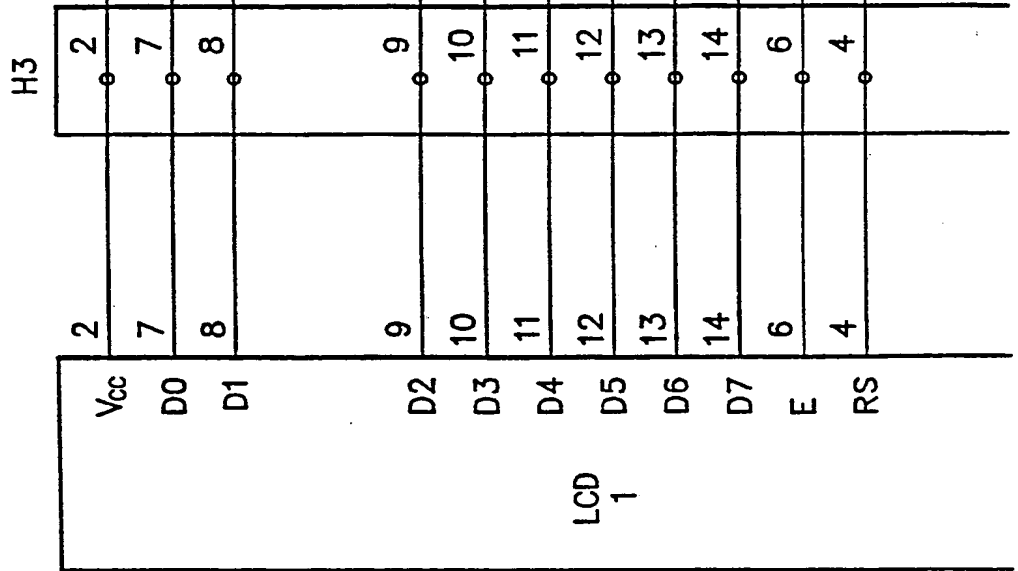
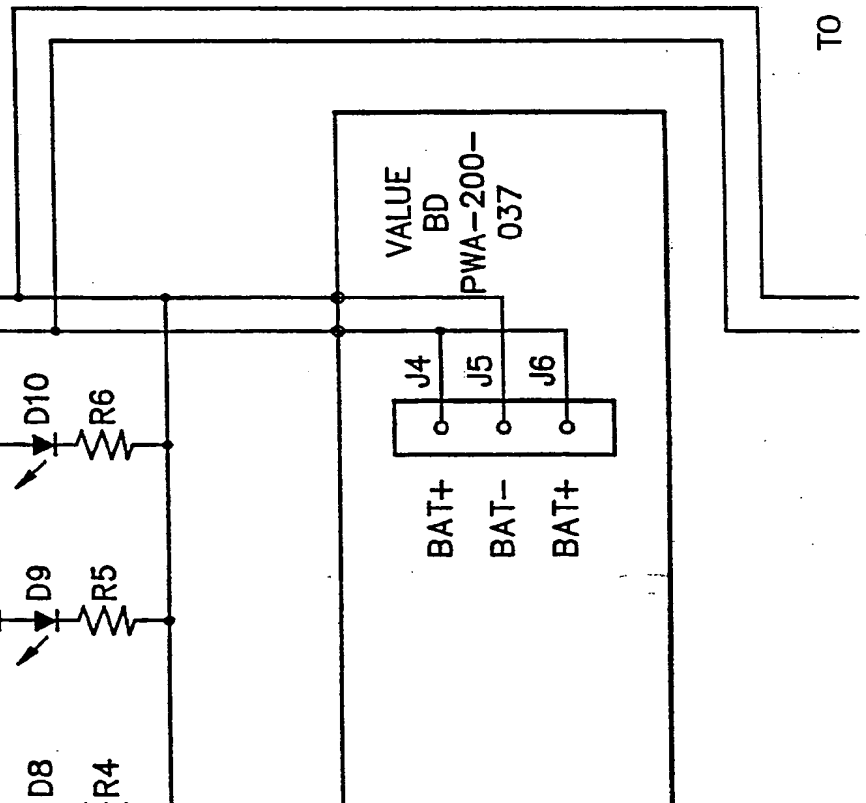
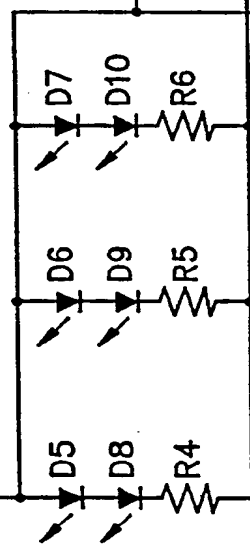
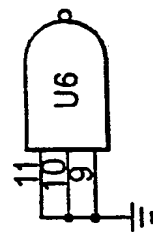


TO FIG. 7d

FIG. 7c

FROM FIG. 7a

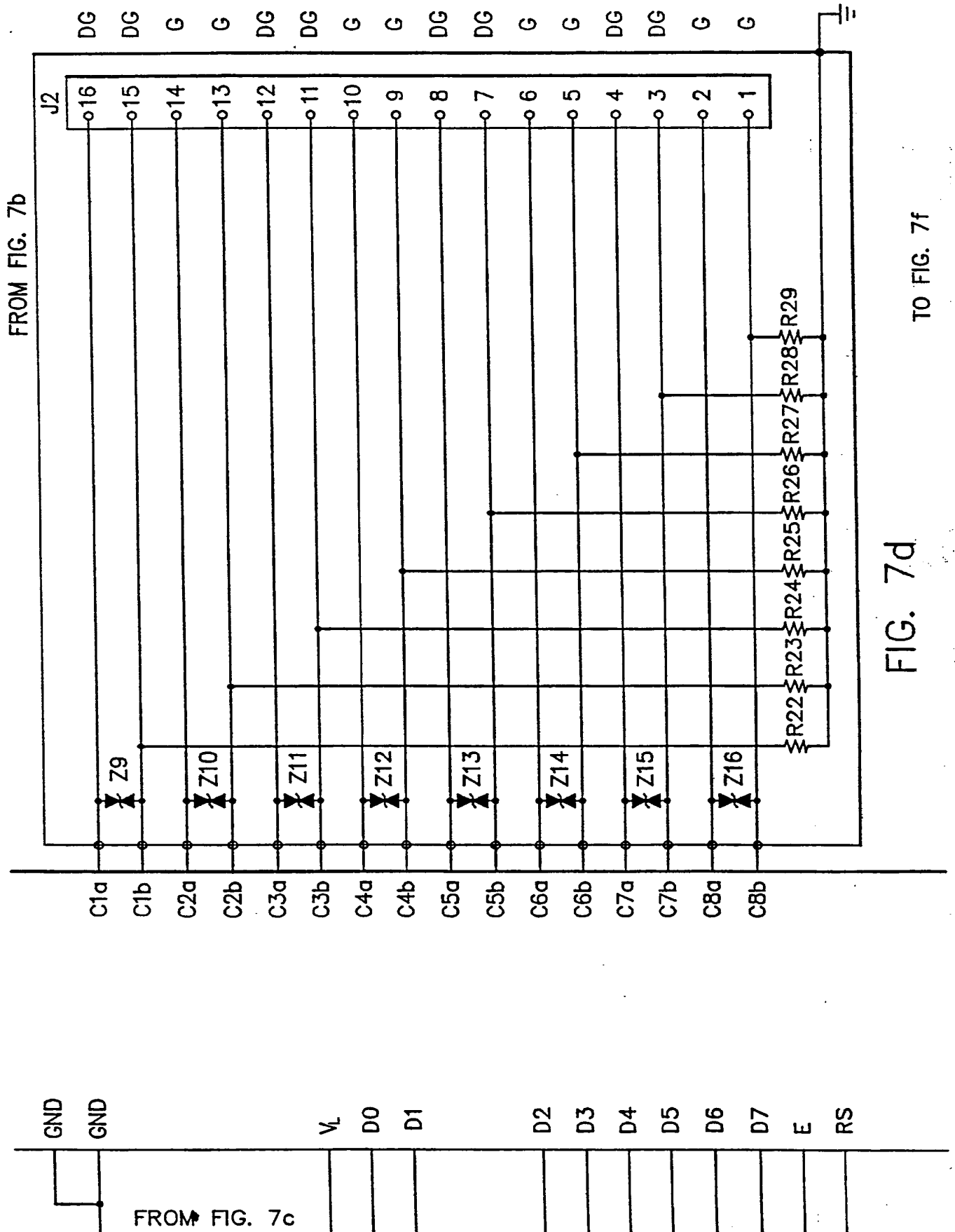
TO FIG. 7d



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TO FIG. 7e

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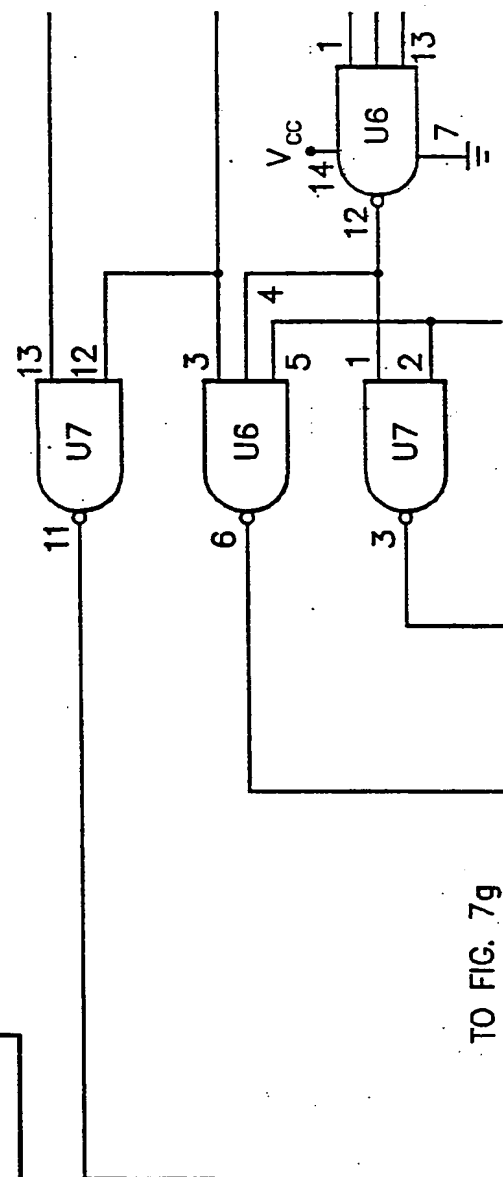
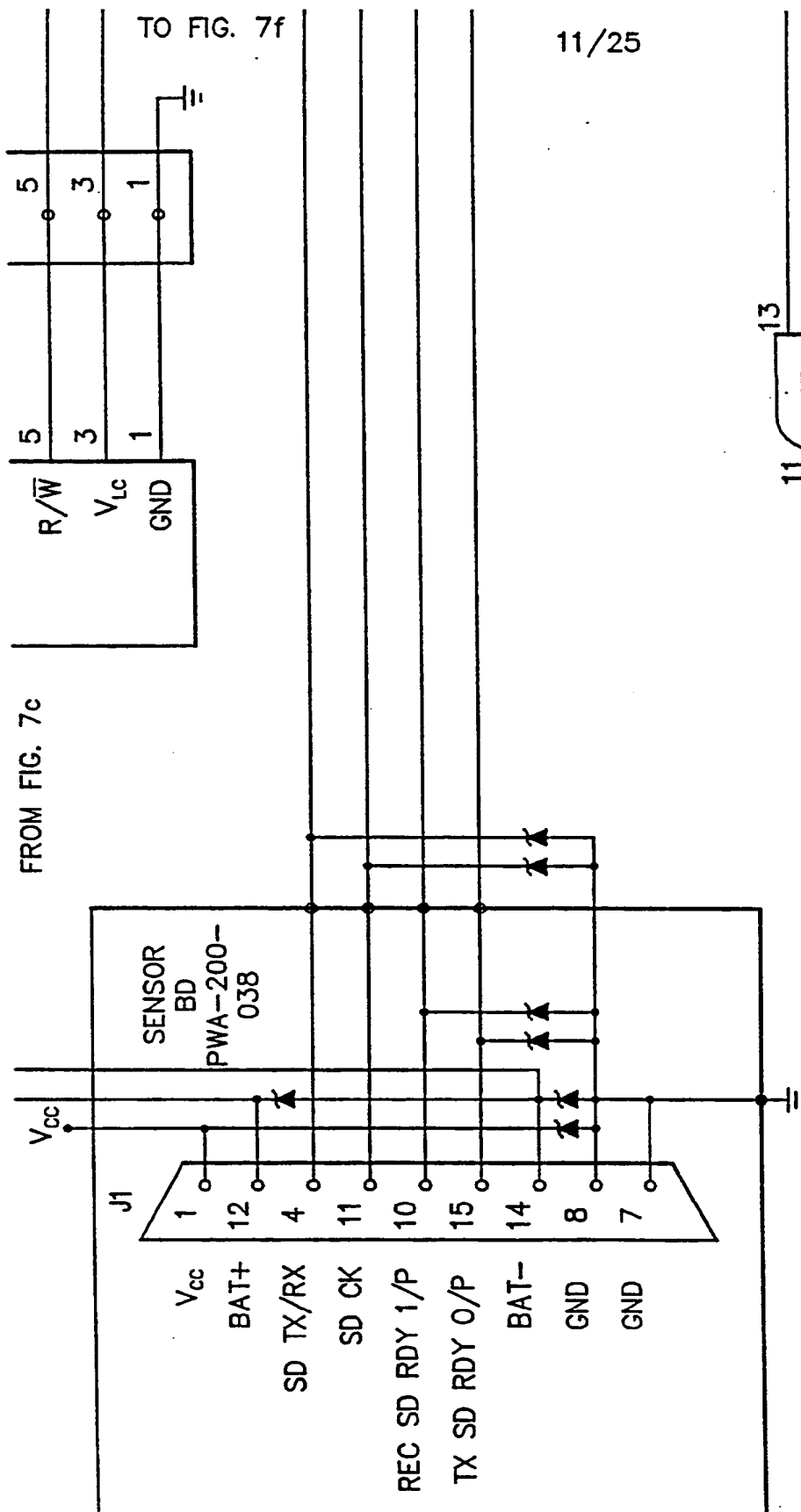
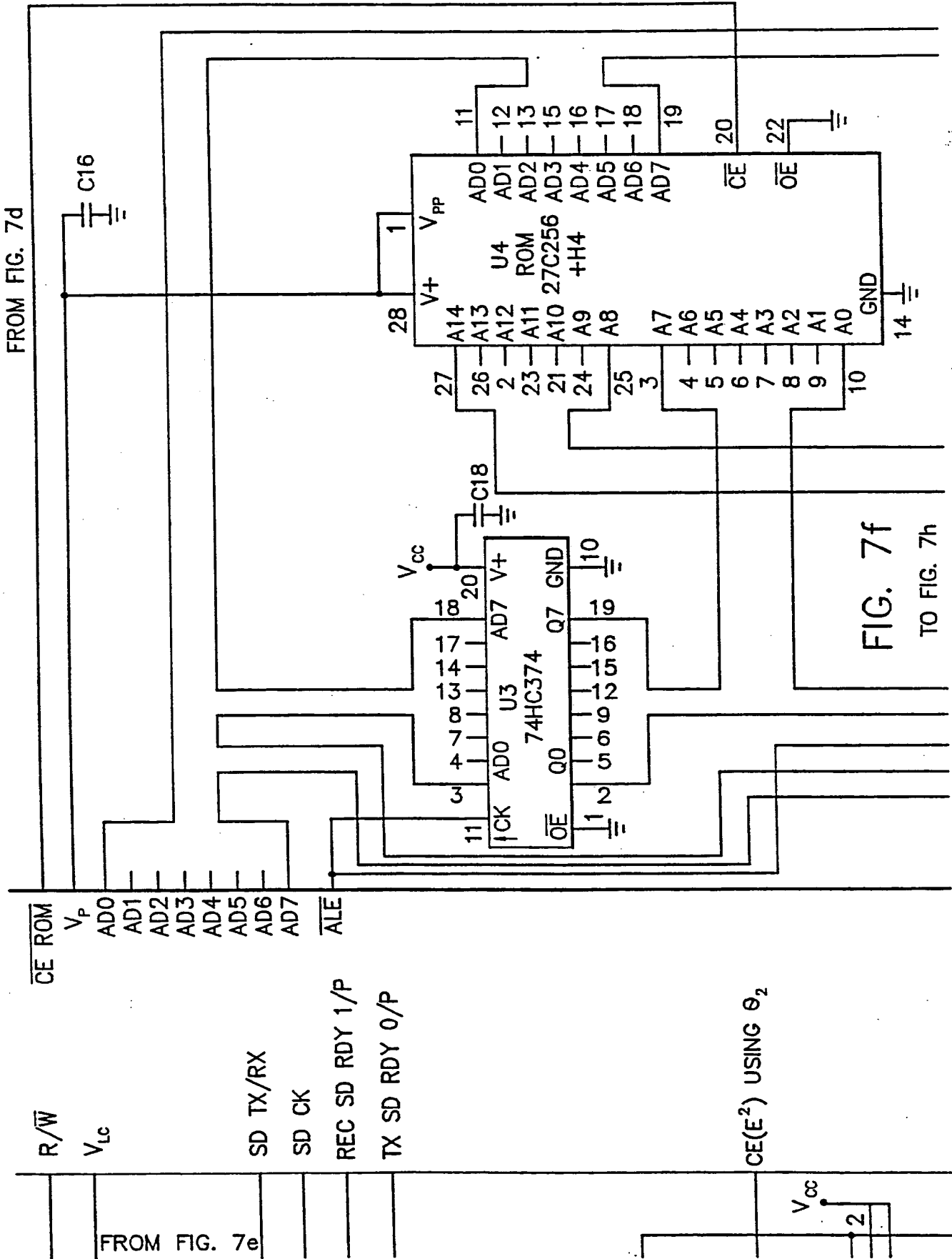
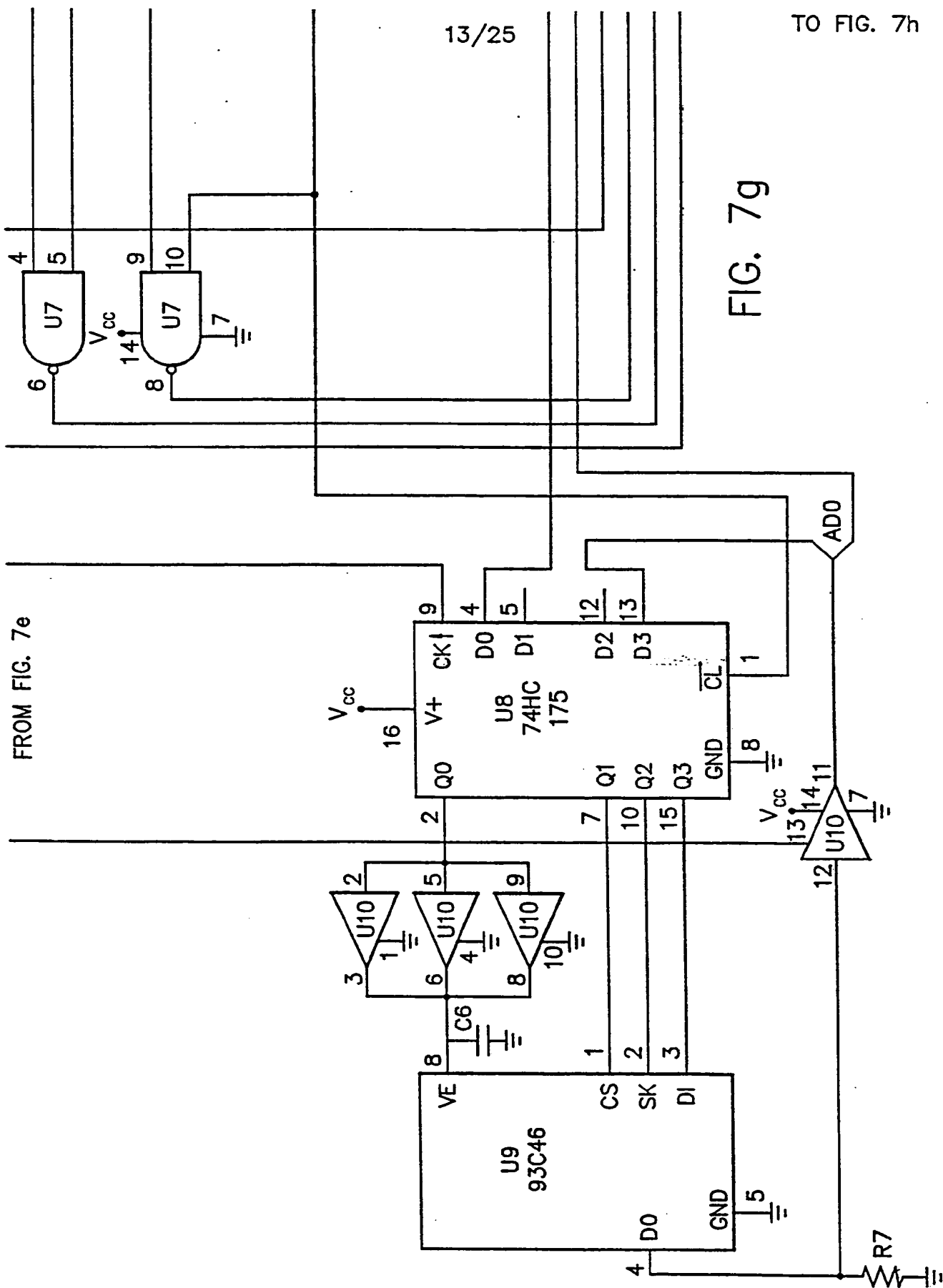


FIG. 7e

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TO FIG. 7h



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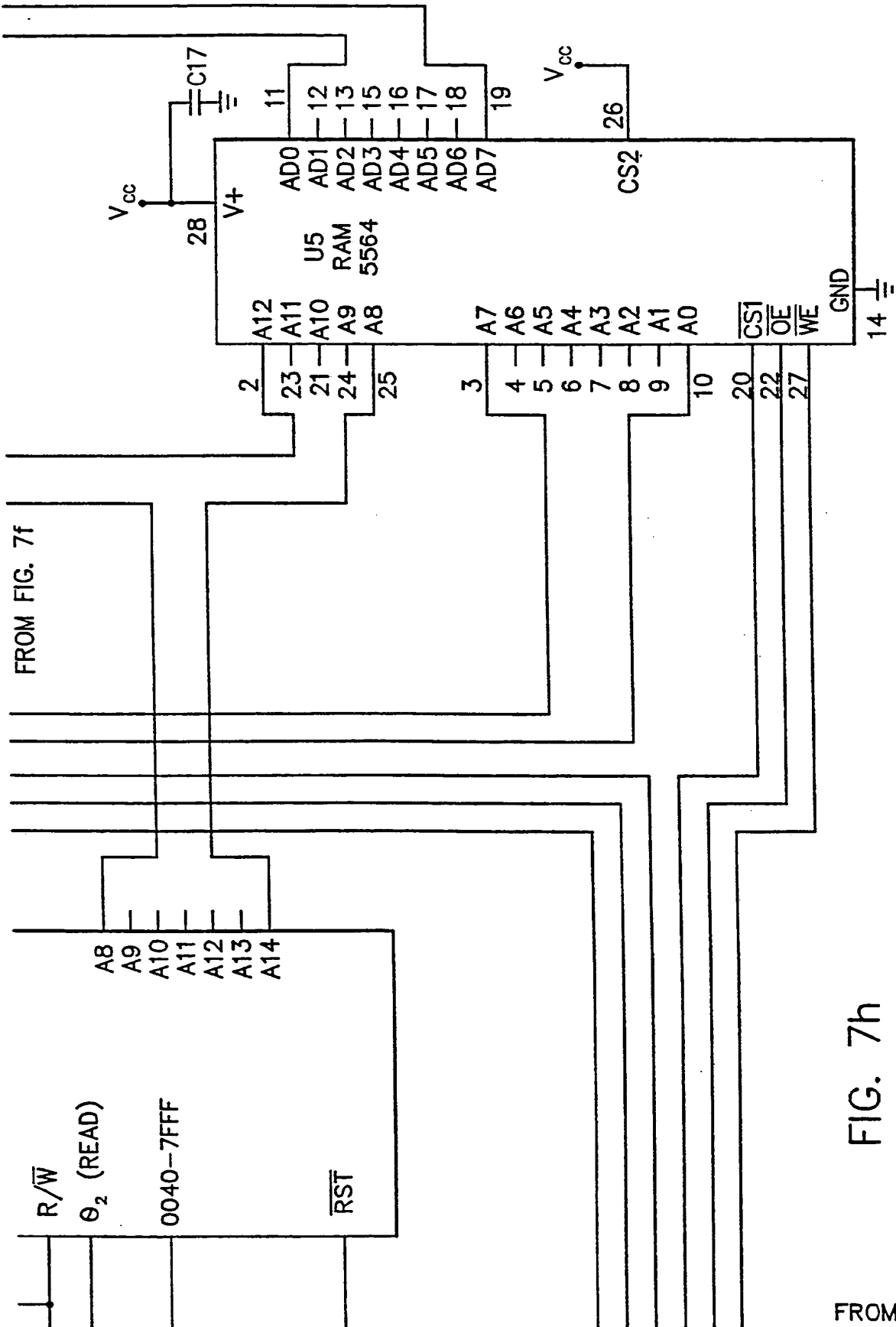
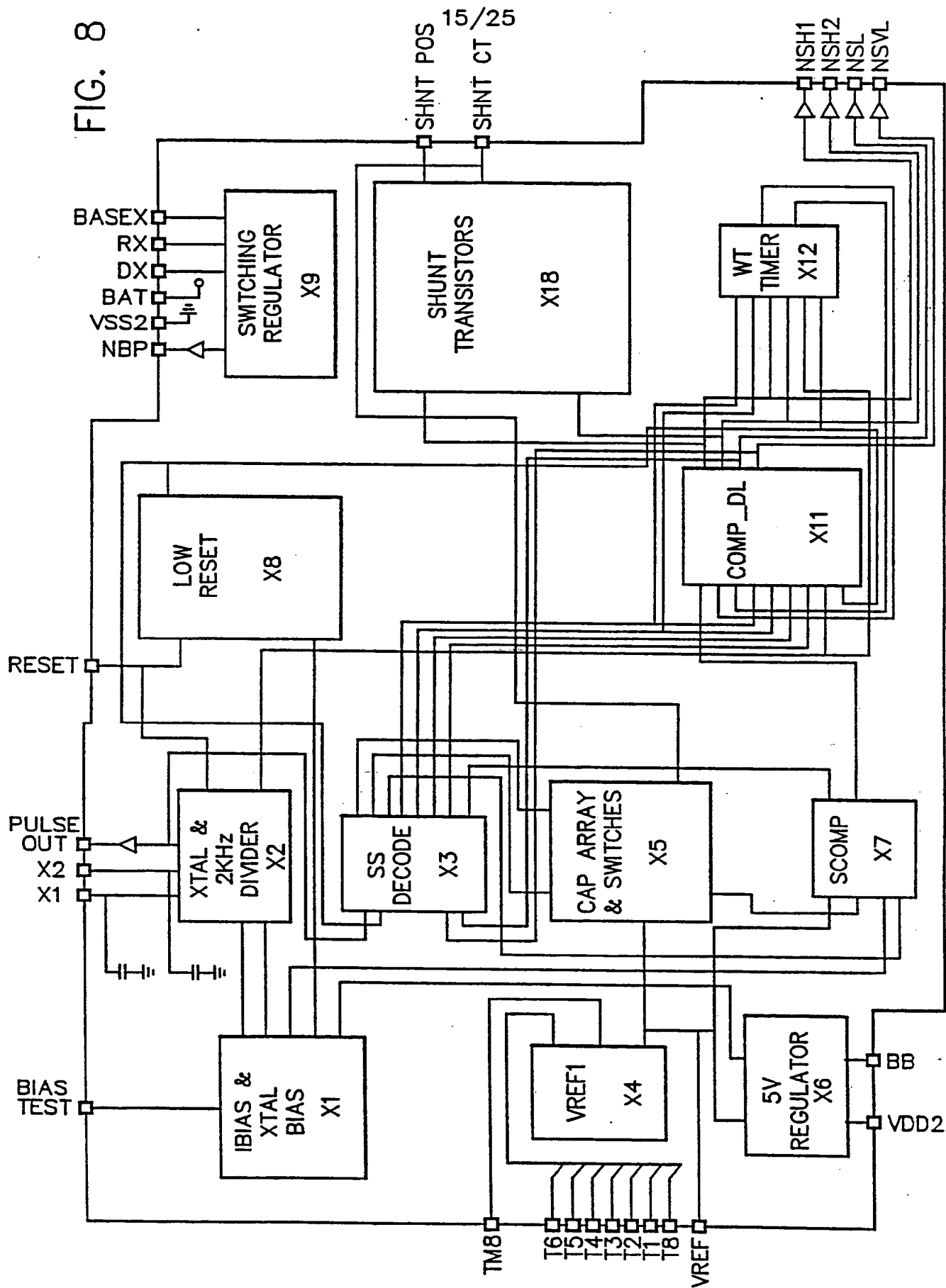


FIG. 7h

FROM FIG. 7g

FIG. 8



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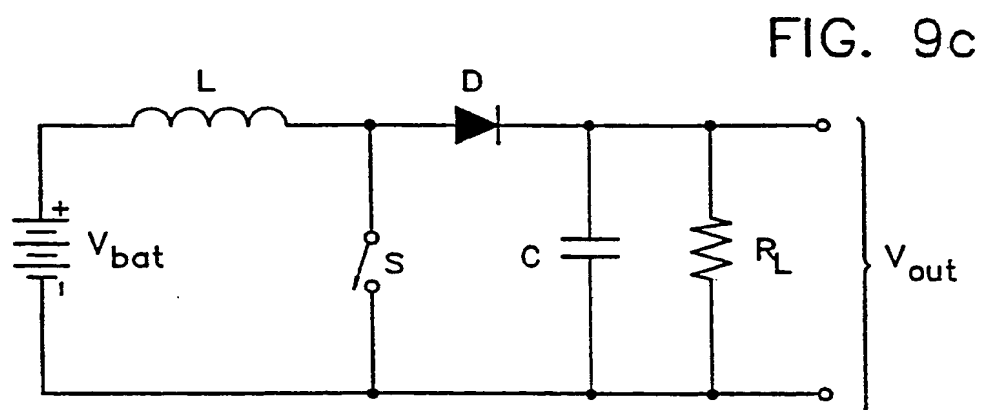
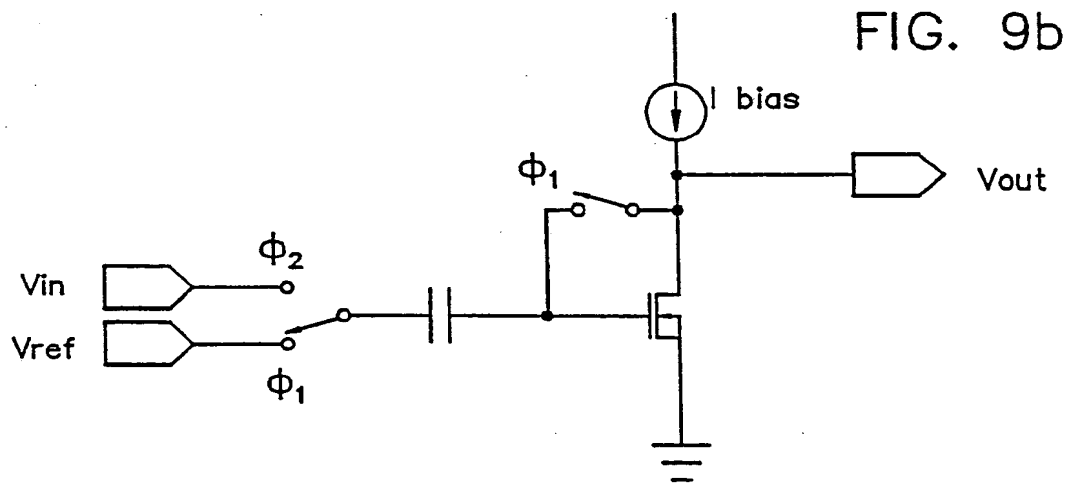
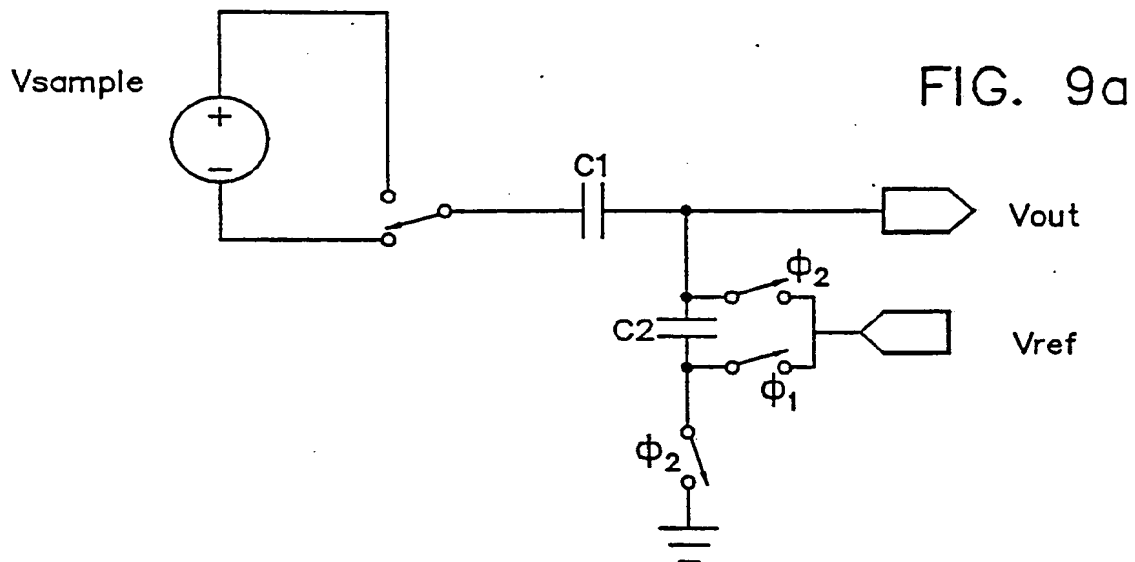


FIG. 10a

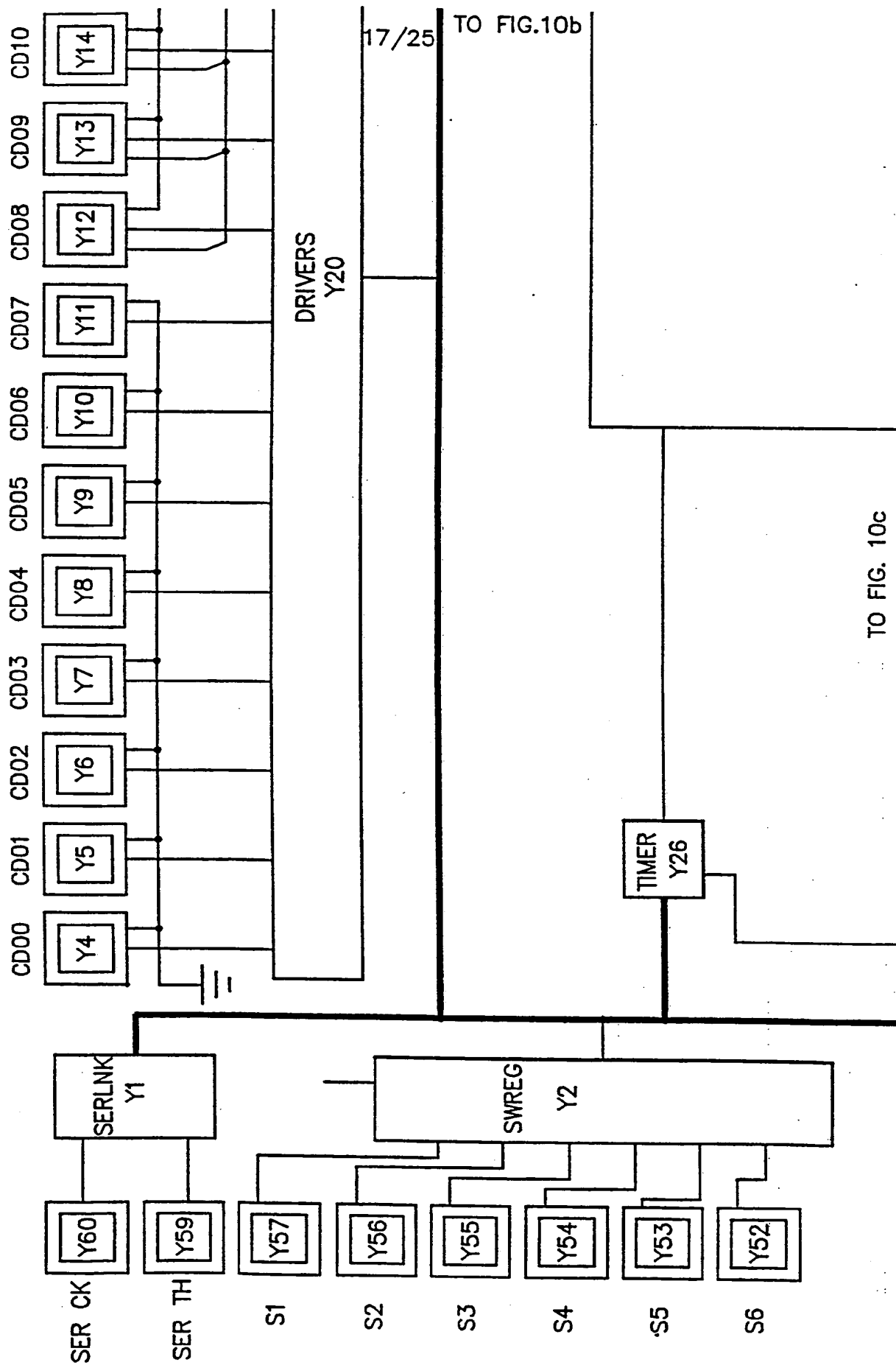
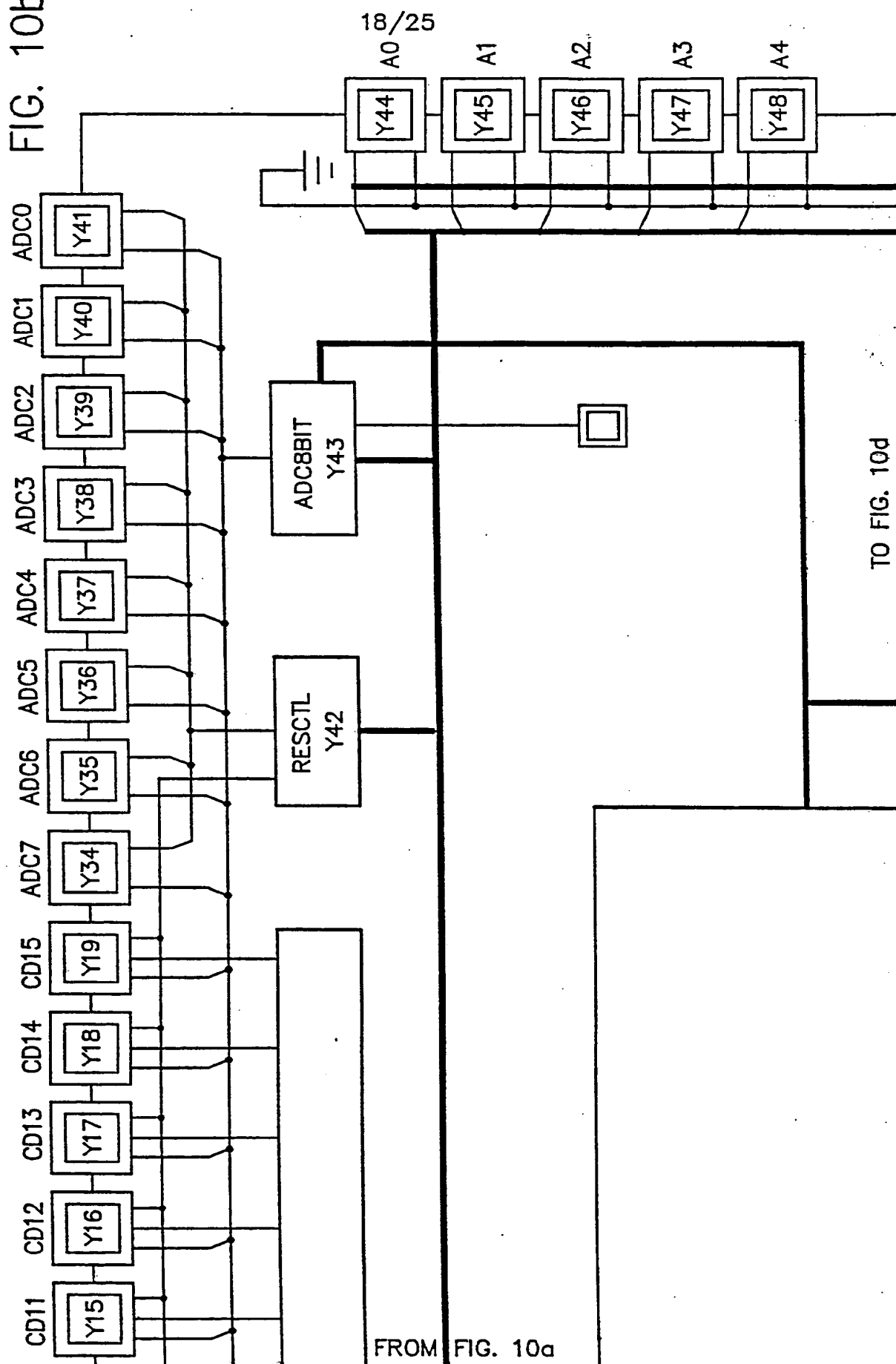


FIG. 10b



TO FIG. 10d

FROM FIG. 10a



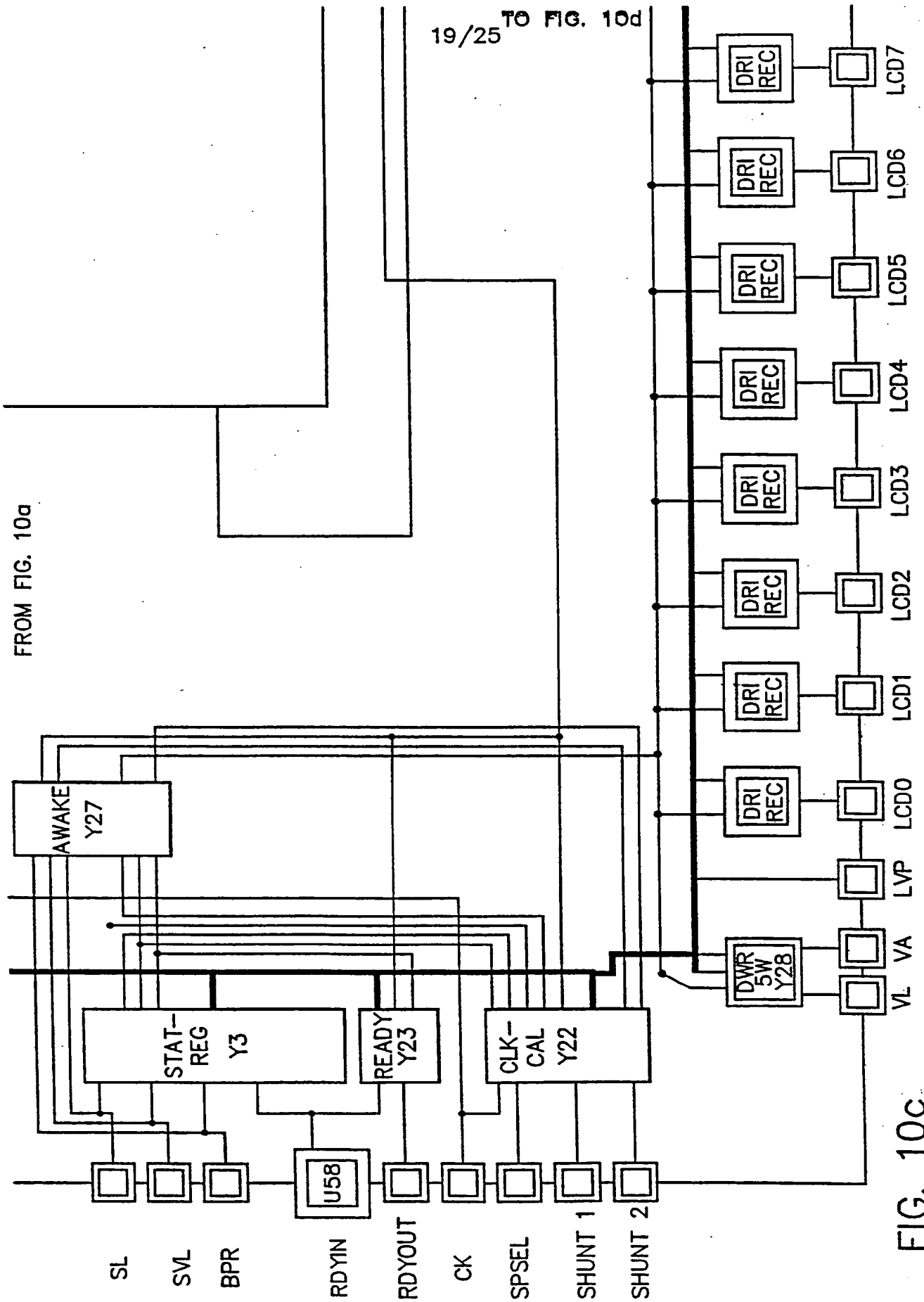
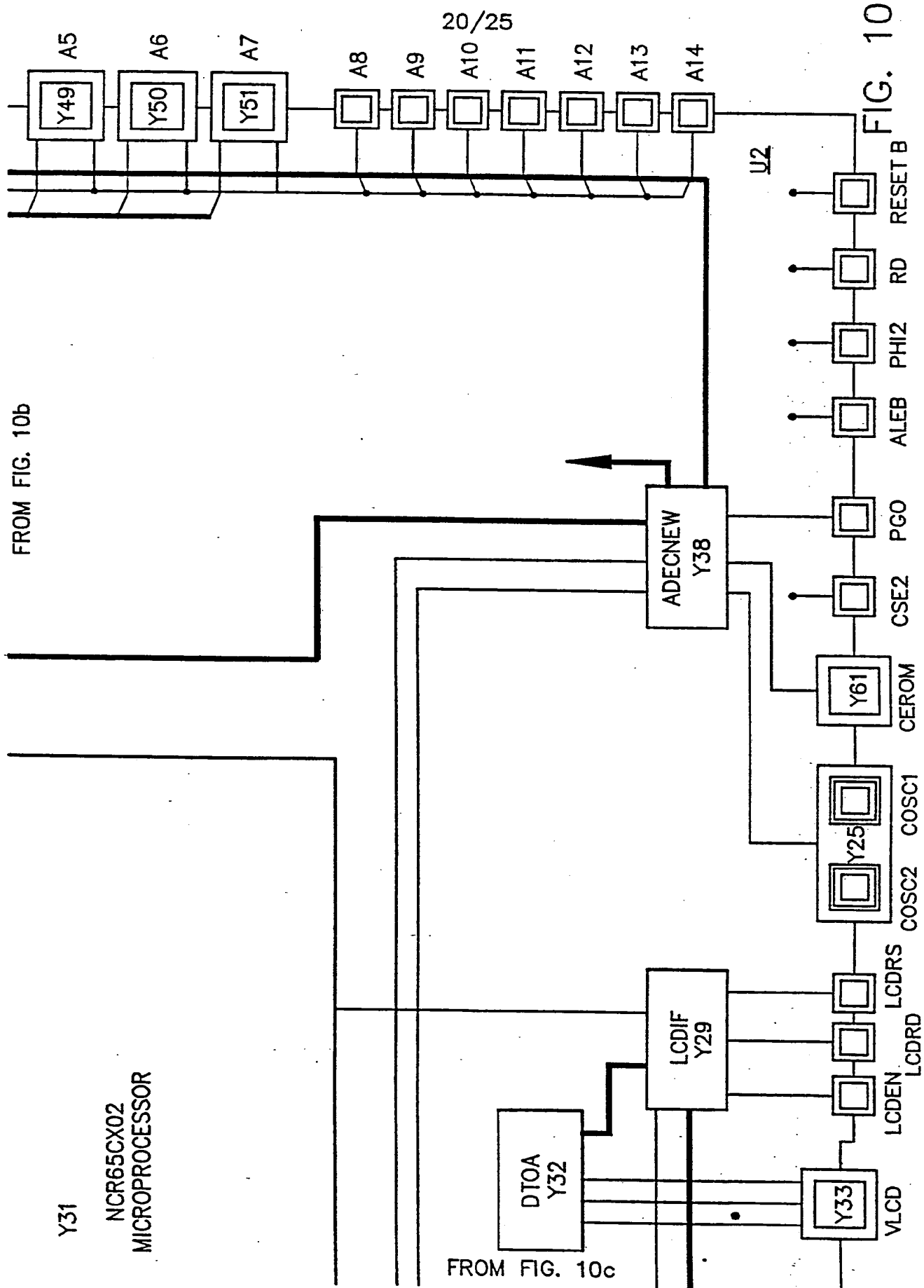


FIG. 10c



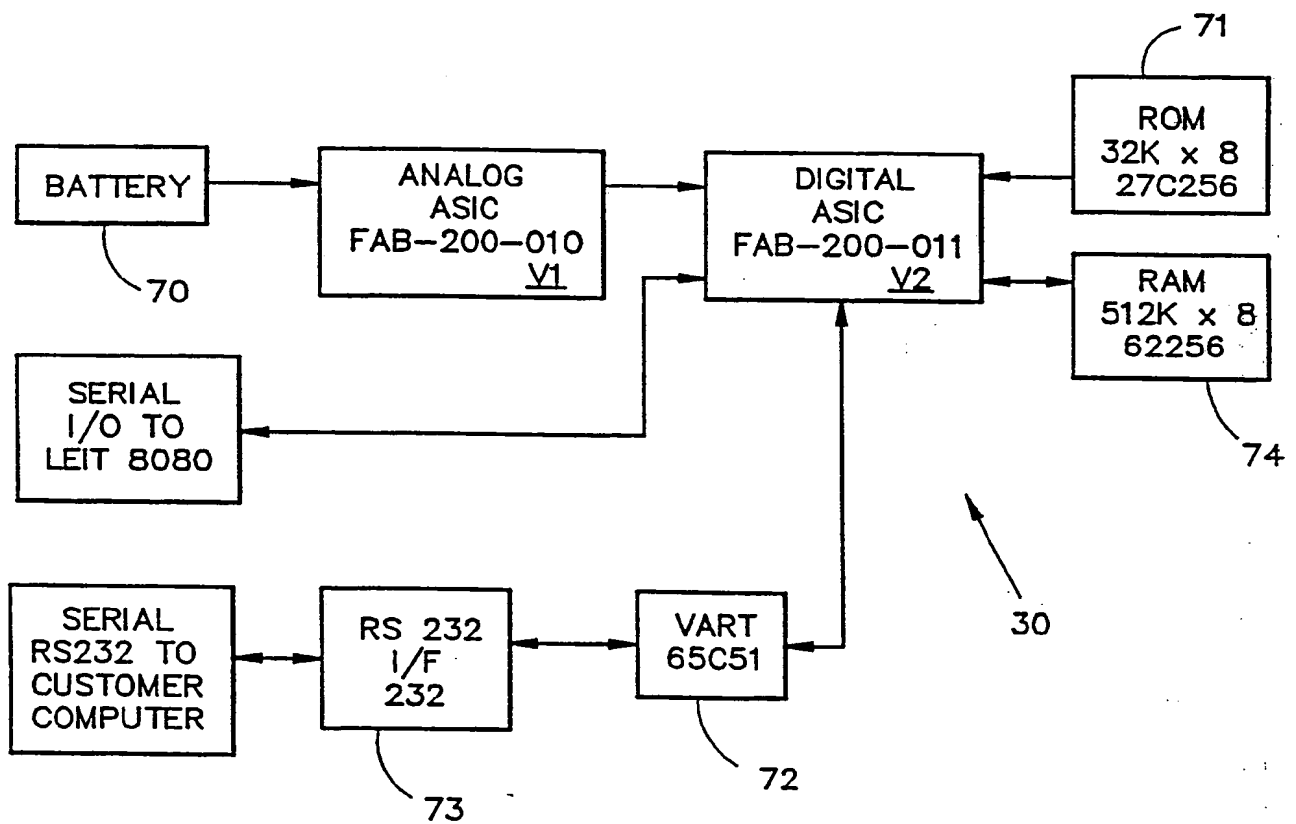


FIG. 11

FIG. 12a

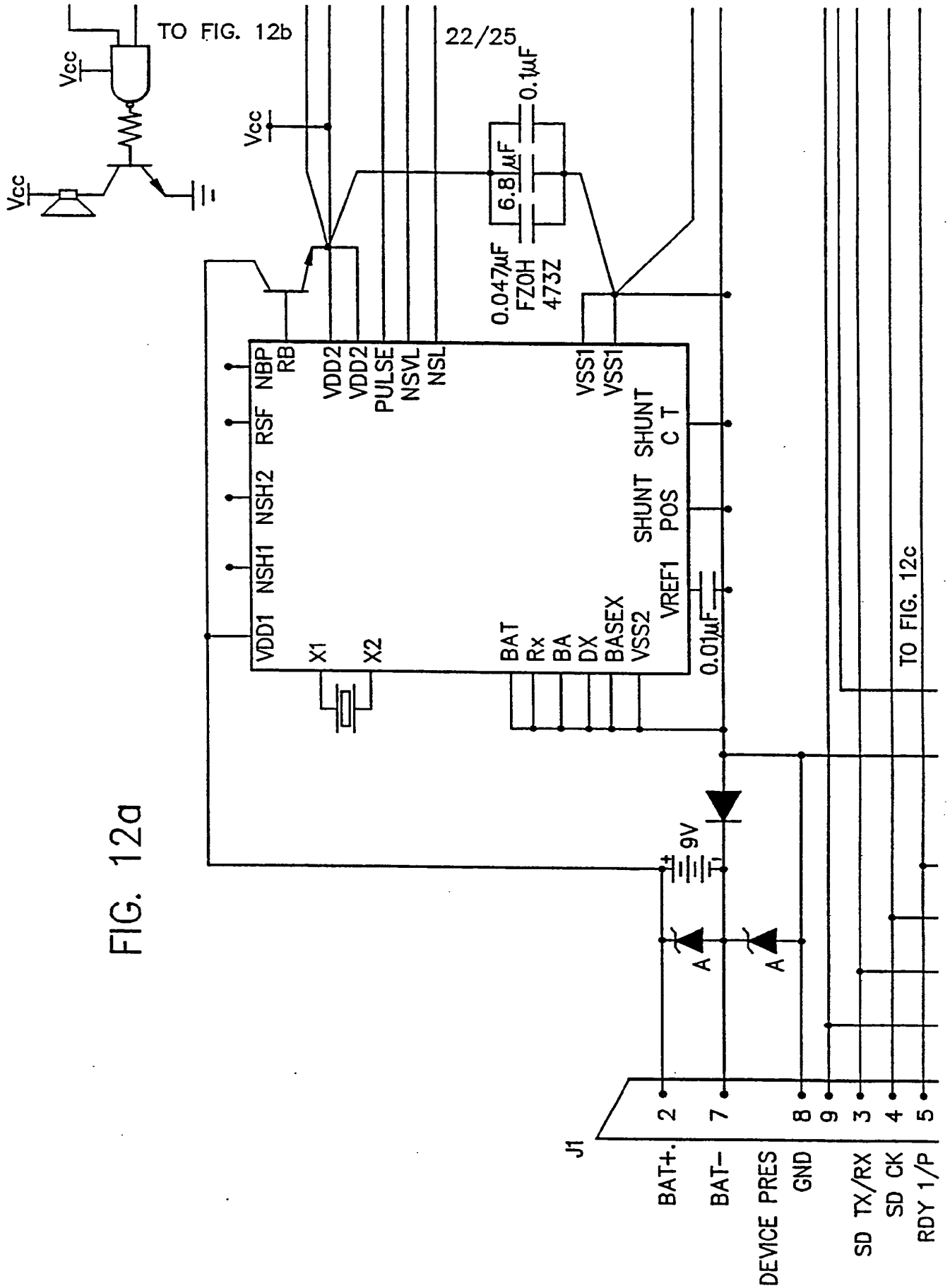
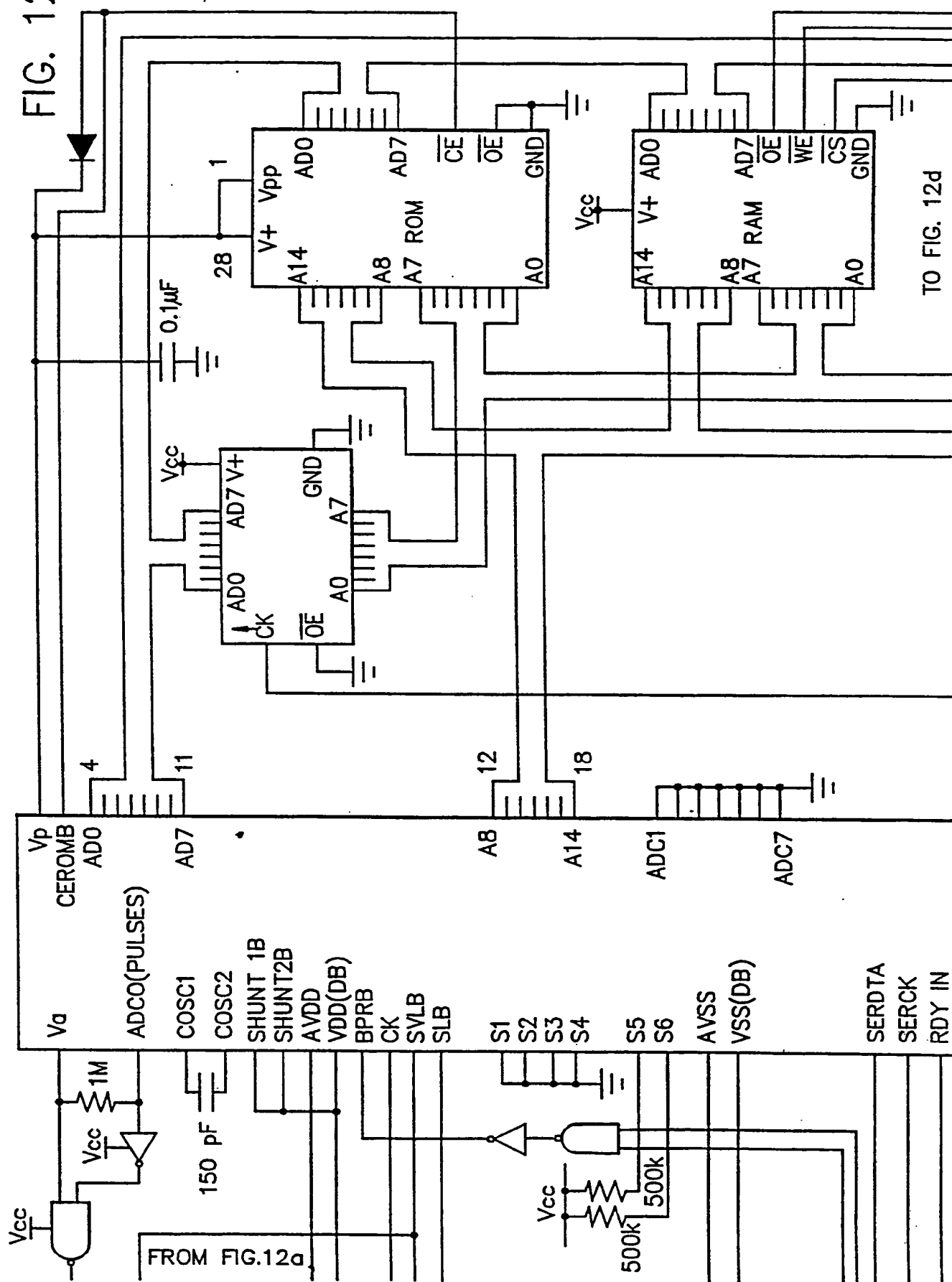
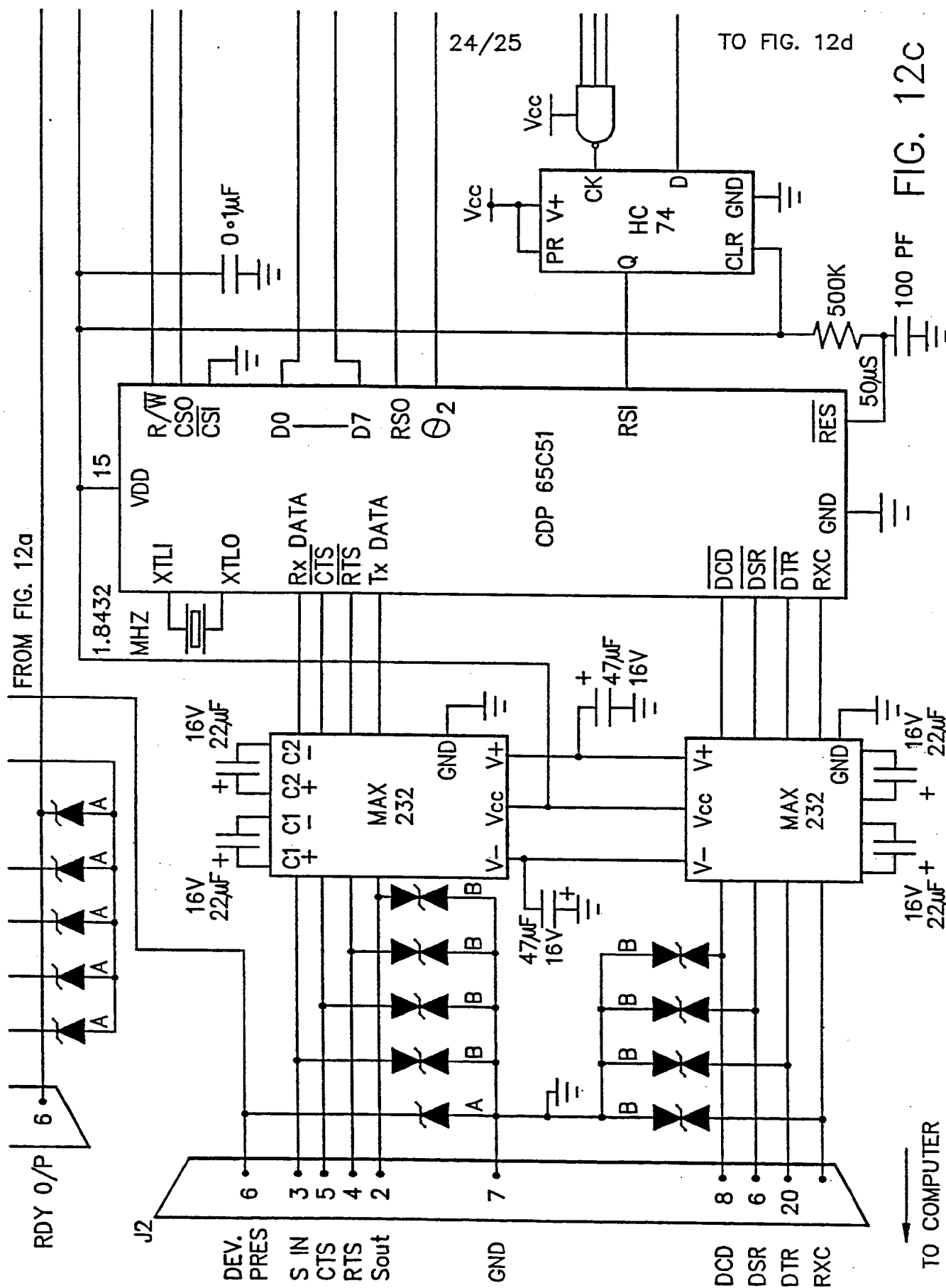


FIG. 12b

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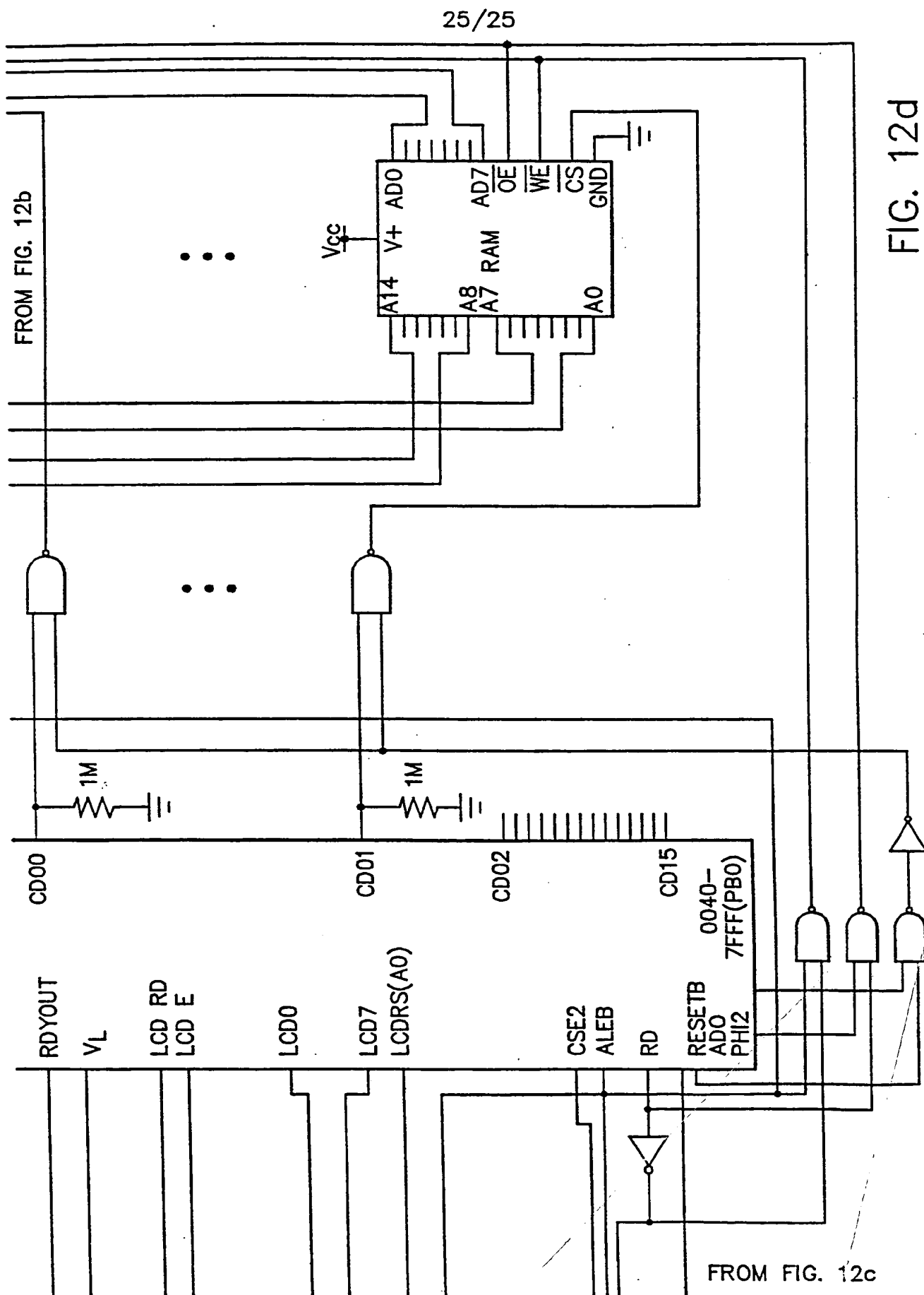


FIG. 12d

# INTERNATIONAL SEARCH REPORT

International Application No. PCT/US89/04403

## I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) \*

According to International Patent Classification (IPC) or to both National Classification and IPC  
 IPC(4): AOIG 25/16  
 U.S. Cl: 364/420

## II. FIELDS SEARCHED

Classification System	Minimum Documentation Searched <sup>7</sup>
	Classification Symbols
U.S.	364/420 239/67, 69, 70

Documentation Searched other than Minimum Documentation  
 to the extent that such Documents are included in the Fields Searched \*

## III. DOCUMENTS CONSIDERED TO BE RELEVANT \*

Category *	Citation of Document, <sup>11</sup> with indication, where appropriate, of the relevant passages <sup>12</sup>	Relevant to Claim No. <sup>13</sup>
Y	WO, A, WO86/05945 (TOWNSON ET AL.) 23 October 1986, see entire document	1, 8, 9
Y	US, A, 4,648,066 (PITT) 3 March 1987, see entire document	1, 8, 9
A	JP, A, 60-164870 (KAWAMURA) 27 August 1985, see entire document	10
A	US, A, 4,722,478 (FLETCHER ET AL.) 2 February 1988, see entire document, see especially fig. 12	11, 12

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### \* Special categories of cited documents: <sup>14</sup>

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

- "&" document member of the same patent family

## IV. CERTIFICATION

Date of the Actual Completion of the International Search

14 DECEMBER 1989

Date of Mailing of this International Search Report

18 JAN 1990

International Searching Authority

ISA/US

Signature of Authorized Officer

David Hunzley